TPS659x0 Silicon Errata

This errata document is common for the TPS659xx family of devices (TPS65950, TPS65930, and TPS65920). The following errata apply to the modules present in the respective devices; for example, the audio errata do not apply to the TPS65920 because the audio module is not present.

Contents

1 32-kHz jitter increase when voice path is on in master mode

Impact:

32-kHz oscillator: 32-kHz clock jitter increase.

Description:

In all I/O buffers, analog ground was shorted with digital ground via charge device model (CDM).

- When voice path is off: 32K cycle jitter short-term peak-to-peak is about 17 ns.
- When voice path is active:
  - Voice sampling rate 8 kHz: Cycle jitter short-term peak-to-peak is about 36 ns.
  - Voice sampling rate 16 kHz: Cycle jitter short-term peak-to-peak is about 31 ns.

Workaround:

None

2 Pop noise on headset output while using 5-wire connection

Impact:

Audio: Pop noise on headset output in 5-wire connection

Description:

Pop noise is heard on headset in 5-wire connection because HSO and HSOVMID amplifiers cannot be switched on at the same time. The enable bits for these amplifiers are in different registers.

Workaround:

Software: In 5-wire configuration, pop noise is reduced by changing register sequencing as follows:

- Power-up:
  - VMID_EN = 1
  - RAMP_EN = 1
  - HS amplifier enabled
  - HSOVMID amplifier enabled
- Power-down:
  - HSOVMID amplifier disabled
  - HS amplifier disabled
  - RAMP_EN = 0
  - VMID_EN = 0

3 Audio: I2S interface timings issue for OMAP2430 and OMAP3430 ES1.0

Impact:

Impact is 1 negative bit shift: (MSB – 1) becomes MSB on McBSP data (TPS659x0 data in)

- If data is less than –6 dBFs → gain of +6 dB.
- If data is equal or higher than –6 dBFs → functionality loss.

Description:

Audio I2S interface, if:

- TPS659x0 Master, I2S mode
- TPS659x0 I2S communicates with a McBSP of OMAP2430 or OMAP3430 ES1.0 (fixed for OMAP3430 ES2.0 in McBSP).

By default, McBSP is in half-cycle mode; that is, received data is synchronous with the rising edge of the clock,and transmission of data is synchronous with the falling edge of the clock. On TPS659x0 side, transmit and receive data occur on the rising edge of the clock.

- Mismatch between implementations

TPS659x0 output buffers for clock and frame synchronization (FS) are not the same so rising and falling edges are sensitive to output loads. This difference added to specification mismatch can affect the functionality for McBSP data transmission, if the FS transition occurs before the clock's falling edge.

Workaround:

Software: On McBSP side, set it in full-cycle mode (transmit with the rising edge of clock) in the PCR_REG register: bit [1] = CLKXP = 0 instead of 1. TPS659x0 register settings do not change.

4 VBUS/VAC unplug debounce time (1*50 ms) not seen when VBAT < 2.6 V

Impact:

BCI: VBUS unplug debounce time (1*50 ms) not effective if VBAT < 2.6 V. No functional impact.

Description:

If VBAT < 2.6 V, then precharge is stopped directly on VBUS unplug with no delay (from normal debouncing logic). Precharge FSM is supplied by VRPRECH, which is switched off at VBUS unplug. Depending on VRPRECH output falling time the debouncing logic may reset. If it is not reset, then precharge is stopped after 50 ms (debouncing time). Due to this behavior of VRPRECH the debouncing time may vary from 50 to 100 ms.

Workaround:

No design change.

5 USB: Cross-over voltage in LS mode is out of spec

Impact:

USB OTG HOST LS cross-over voltage is out of spec. This could lead to not recognizing the USB driver connected on DP/DM.

Description:

Low-speed (LS) cross-over voltage is defined in USB standard from 1.3 and 2.0 V for a capacitance of from 200 to 600 pF in LS. In this configuration, cross-over voltage is below 1.3 V.

Workaround:

The workaround depends on the use-case:

- If used as standard host → LS is mandatory and the following software workaround should be used for certification.
- If used as OTG → LS compliancy is optional, then it will depend on the target peripheral list defined for this application. If any targeted peripheral is an LS-only device, then use the software workaround.
- If used as device-only → not required to be LS compliant.

Software workaround:

- Set VUSB_3P1 at 3.4 V.
- Set PROTECT_KEY register (add 0x0000 0044) to 0xC0.
- Set PROTECT_KEY register to 0x0C.
- Set TRIM1 register (add 0x0000 006F) bits <5:4> to 11.
- Set PROTECT_KEY register to 0x00.

6 I/O: CLK256FS potential reflection issue

Impact:

I2S: Audio issue if used in slave mode with CLK256FS as synchronization signal.

Description:

Synchronization with CLK256FS between McBSP master (OMAP) and TPS659x0 (I2S slave) can be problematic due to a glitch on CLK256FS.

I/O buffer strength makes potential reflection issue on the line depending on its delay and also on the capacitance connected at the far-end. The solution is to increase the impedance of the I/O buffer by adding serial resistance.

Workaround:

Hardware workaround: A series resistor of 33 Ω can be added on optimized PCB to minimize reflection effect.

7 BCI: USB charge stopped by BCI watchdog

Impact:

USB BCI automatic charge may be stopped by the BCI watchdog.

Description:

USB automatic charge may be stopped inopportunely by the BCI watchdog. This BCI reset (no charging) happens on QC1 only for USB automatic charge.

Workaround:

Software: Disable the MADC watchdog at charge startup and enable it when a correct state is achieved in the state-machine. State monitoring can be performed by using interrupts.

Unmask BCI interrupt PIH_ISR2 in the PIH_ISR_P1 register and ICHGLOW_ISR1 in the BCIISR1A register.
Set BCIMFKEY to 0x6D to unlock the BCIMFTH3 register.
Set BCIMFTH3 bit ITBCIGROUP to 0 and bit ITBCIFSM to 1 to allow interrupts on state change in the ICHGSLOW_ISR1 status bit.

After enabling the charge by setting the USBFASTMCHG bit to 1 in the BCIMTST4 register:
If a BCI main charge state change interrupt is triggered in the PIH_ISR2 bit of the PIH_ISR_P1 register and in the ICHGSLOW_ISR1 bit of the BCIISR1A register and if the current state is quick charge USB 1 (RDSLSTATEC = 010010 in the BCIMSTATEC register),

Then write BCIMFEN4 = 0x60 to disable the MADC watchdog.

If another state change interrupt is triggered and if the state is changed to quick charge USB 2 (RDSLSTATEC = 010011),

Then write BCIMFEN4 = 0x68 to enable the MADC watchdog.

8 Audio: SW McBSP patch for TDM mode

Impact:

Audio I2S interface, if: → TPS659x0 master, TDM mode

Description:

See item 3: same root cause but different software patch.

Workaround:

The workaround implementation is on OMAP side.
Software: PCR_REG[1] = CLKXP = 1 instead of 0 (set the transmit clock polarity on the falling edge instead of the rising edge). XCR2_REG[1,0] = XDATDLY = 2 instead of 1 (set the bit delay at 2 bits instead of 1).

9 Audio: Drift of HSO THD for high temperature in 4-wire mode

Impact:

Audio: Distortion on headset output for 4-wire mode at high temperature.

Description:

The THD of headset amplifier in 4-wire mode is temperature dependent. THD measured with 0 dB input sine wave is around 6 dB higher at high temperature (125 degrees) than maximum specification (–75 dB).

Workaround:

Minor impact: None

10 USB: OTG SRP VBUS PU value

Impact:

USB: USB OTG SRP PU timer window limitation.

Description:

Maximum specification has been increased to 3 kΩ for lower voltage value of VBUS, limiting charge current and timing window.

Workaround:

This workaround implementation is on OMAP side. The workaround is to set in the OMAP OTG controller a SRP VBUS pulsing charge timer setting in the range from 36 to 60 ms. This aligns the OMAP and TPS659x0 timer windows.

11 USB: USB full-speed 4-pin serial mode limitation

Impact:

USB: In full speed 4-pin serial mode it is possible that data communication error occurs depending on data line jitter due to number of HUBs in series.

Description:

Proper communication cannot be assured for more than 1 HUB in FS serial mode 4 pins. Standard specifies a maximum allowable data line jitter. TPS659x0 plus 1 HUB plus OMAP controller consumes 100 percent of data line jitter budget.

Workaround:

No design fix. The 4-pin serial mode is recommended not to be used.

12 USB: Increased error rate due to HS calibration comparators continuous toggle

Impact:

USB: potential HS error rate increase due to HS calibration fault.

Description:

There is a theoretical probability that from time to time, HS calibration loop erroneously calibrates the 45-Ω termination. As this loop runs continuously, it automatically recovers but only for a short period of time, and it could generate a communication error. The root cause is due to signal corner conditions.

Workaround:

None needed. This issue has only been highlighted during simulation and the probable occurrence on silicon is extremely low. If this error condition occurs, then the higher level USB protocol recovers naturally.

13 Battery unplug and replug in slave mode

Impact:

Incorrect boot value during next powerup, VDD1 and VDD2 could have incorrect default voltage value, LDOs can remain enabled, and configuration register can be corrupted.

Description:

In the case of battery removal to reset the device, a 32K clock cycle is needed after the 2.1-V VBAT low threshold detection. In slave mode, if the external master device detects battery low before this and cutoffs the 32K clock, then the internal power-on reset (POR) is not effective.

If the battery is removed, the battery voltage falls, then the power configuration registers start to corrupt (VRRTC power domain is not high enough to secure data retention). At this point either the VRRTC node falls below 0.3 V and all registers will be reset at no-supply value (and there is no issue), or the battery is plugged back in the device.

If the battery is reinserted before the no-supply reset, then the VRRTC node rises again and the device can powerup with corrupted power configuration register.

Typical failure is observed when the battery is removed and reinserted in a window from 50 and 300 ms.

Workaround:

Add external pulldown circuitry to discharge VBAT or VRRTC node and ensure a proper no-supply state, while VBAT low is detected.

Or secure 32K switch-off by external master and let 32K run during battery removal until the VBAT < 2.1 V is correctly detected by TPS659x0.

14 VIO disable in slave mode

Impact:

Disabling VIO in slave mode is not supported.

Description:

In slave mode, even if the IO_1P8 device power is provided by an external supply instead of VIO, it is not possible to turn off the VIO regulator. This is because the internal clocking of the device uses the RC oscillator of the VIO regulator and disabling the regulator also disables the clock, thus preventing the correct functionality of the device.

Workaround:

VIO can be placed in sleep mode instead of off. The VIO current in sleep mode is 20 μA typical and 50 μA maximum.

15 Audio: AUXR input not functional when ADCMICSEL enabled

Impact:

When the digital microphone interface is enabled by setting ADCMICSEL = 0x0F, the AUXR input is not functional. This also impacts the FM loop mode when AUXR is used.

Description:

When the digital interface is enabled, the internal signal AUXR_EN_CTL_LOWV is in low state. This disables the AUXR input.

Workaround:

None

16 MADC: Drift on MADC offset

Impact:

Incorrect VBAT measurements in the long run.

Description:

VBAT_MADC_OFFSET_2P9V (internal parameter) drifts after 72 hours of burn-in at 140 degrees. This drift can have impacts on device functionality like battery charging.

Workaround:

Always enable the ADC in standby and active mode (MADCON = 1). This increases Iddq by 34 μA in standby.

17 VUSB3V1 VBUS overvoltage debouncer not working when the PHY is powered down

Impact:

There is no functional impact; however, certain conditions must be avoided. Read description and workaround.

Description:

The LDO VUSB3V1 VBUS overvoltage detector is disabled when the PHY is powered down. The maximum VBUS voltage that can be tolerated when PHY is powered down is 5.25 V (USB 2.0 standard maximum VBUS voltage).

Avoid supplying the LDO VUSB3V1 on VBUS if the PHY is powered down. There is a risk that VBUS can rise above USB specified voltage range. The following scenario is unsafe:

LDO VUSB3V1 enabled, supplied on VBUS (VUSB_DEDICATED1/SW2VBUS = 1), with the PHY powered down (PHY_PWR_CTRL/PHYPWD = 1) and VBUS potentially connected to a non-USB compliant device (for example, dedicated charger)

In all other scenarios, the device can accept a VBUS voltage up to the maximum voltage specified in the Data Manual.

Workaround:

- LDO VUSB3V1 enabled, supplied on VBAT (VUSB_DEDICATED1/SW2VBAT = 1)
- LDO VUSB3V1 enabled, supplied on VBUS (VUSB_DEDICATED1/SW2VBUS = 1), with PHY enabled (PHY_PWR_CTRL/PHYPWD = 0)
- LDO VUSB3V1 enabled, supplied on VBUS (VUSB_DEDICATED1/SW2VBUS = 1), with PHY suspended (PHY_PWR_CTRL/PHYPWD = 0 and FUNC_CTRL/SUSPENDM = 0)
- LDO VUSB3V1 enabled, supplied on VBUS (VUSB_DEDICATED1/SW2VBUS = 1), with PHY powered down (PHY_PWR_CTRL/PHYPWD = 1) and VBUS only connected to USB-compliant devices

18 In-band tone in ADC path when Fs = 32 kHz and MCLK = 19.2 or 38.4 MHz

Impact:

No functional impact

Description:

~5 kHz to 9 kHz tone at about –80 dBFs in uplink path is present when the sampling rate is 32 kHz and when the master clock is 19.2 or 38.4 MHz. No issue when master clock is 26 MHz.

Workaround:

None

19 Leakage between 32KXIN pad and ground path

Impact:

There will be some leakage between 32KXIN and ground paths based on the input voltage applied.

Description:

When the crystal oscillator is in the bypass mode, the 32KXIN input pad should be in high-impedance mode. However, this is not the case. This allows a leakage path between this pad and ground. The following table shows the relation between the input voltage and the leakage.

	Input Impedance (kΩ) From Ground		Input Leakage (μA) To Ground	
Input Voltage (V)	**Minimum**	**Maximum**	**Minimum**	**Maximum**
<0.4	>10,000	>10,000	0.0	0.0
0.6	2960	>10,000	0.0	0.2
0.8	700	3550	0.1	1.2
1.0	350	530	1.8	2.9
1.2	180	330	3.7	6.3
1.4	120	240	6.1	10.8
1.6	90	190	8.8	15.8
1.8	70	160	12.1	21.5

Workaround:

None

20 Soft volume limitation

Impact:

Soft volume limitation

Description:

Soft volume control feature cannot be used under specific register settings. When bit SOFTVOL_EN = 1 and OPT_MODE = 1, the user cannot use soft volume feature and cannot control the fine gain settings.

Workaround:

This table shows when soft volume can function and when it cannot.

Register OPTION = 0x02				Register RX_PATH_SEL		Can Soft Volume Work?
ARXR2_EN	**ARXL2_EN**	**ARXR1_EN**	**ARXL1_VRX_EN**	**RXL1_SEL**	**RXR1_SEL**	
1	1	0	0	0x0 or 0x1	0x0 or 0x1	No
1	1	0	0	0x2 or 0x3	0x2 or 0x3	Yes

21 Reduced DCDC efficiency on TPS65930/20

Impact:

Switcher efficiency for TPS65930/20 is lower when the device powers up with default drive setting.

Description:

VDD1, VDD2, and VIO have an unexpected efficiency degradation in PSM/PWM modes at high load currents (>500 mA) due to an effect linked to the packaging parasitics. Changing the drive of the switcher from the default setting to the minimum drive strength recovers the efficiency performance. A similar effect is seen on the efficiency measurements of VDD1 in PFM mode. Again, changing the drive of the switcher from the default setting to the minimum drive strength recovers the efficiency performance. No issues have been reported on the efficiency performance of VIO and VDD2 in PFM mode. Changing the drive to its minimum strength on either of these two switchers has no impact, positive or negative, on the efficiency.

Workaround:

Programming the drive strength to its minimum level to achieve normal efficiency performance in all modes for the switchers can be achieved by setting the DRIVE_SEL bits for the appropriate MISC_CFG switcher register to the value 101 at boot.

22 PWR: Device turns ON due to PWRON edge detection when it actually should not turn ON.

Impact:

Device turns ON when not expected to be ON.

Description:

When the battery is plugged for the first time the device powers up by default. If the STARTON_VBAT bit is set to 0 then the device does not power on when battery is inserted.

However, if the battery is removed followed by the PWRON switch (connected to the PWRON pad) shorted to GND and then the battery is plugged back in, the device will power ON.

During the above sequence of operation the internal debouncer is out-of-reset and a battery plug event is seen as an edge, thus triggering a power ON event.

Workaround:

None.

23 PWR: Device switches OFF after 8-second restart event if the STOPON_PWRON register bit is set after device restarts.

Impact:

Device will poweroff unexpectedly.

Description:

If the STOPON_PWRON bit is set to enable the 8-second PWRON press restart event, then the device should restart and normal behavior should resume. However, if the STOPON_PWRON bit is written in the 8-second window immediately following the restart then the device powers off.

Workaround:

None.

24 I^2C high-speed limitation to 2.2 MHz due to hold time issue

Impact:

Due to higher I^2C data hold time in HS mode, there is a frequency limitation in HS mode.

Description:

I²C data hold time in HS mode is higher than the specification when reading I²C registers. This leads to a data setup issue, which introduces a frequency limitation in HS mode (cannot reach 3.4 MHz as specified in I²C standard).

The limitation is for the control I²C. The limitation is also for SmartReflex I²C only when used with products other than OMAP35xx with SmartReflex. HS mode works correctly for SmartReflex I²C when using OMAP35xx.

System Clock for TWL5031	SR I²C Using OMAP35xx	Control I²C
19.2 MHz	HS mode OK	HS mode maximum is 2.2 MHz
26 MHz	HS mode OK	HS mode maximum is 2.4 MHz
38.4 MHz	HS mode OK	HS mode maximum is 2.9 MHz

Configuring the communication speeds to higher than the maximum limits listed for the control I²C could lead to errors on the interface, and is therefore not allowed. This is due to the fact that the hold timing violation has as a consequence a data setup violation that leads to a possible bad read data sampling.

Workaround:

None.

25 HFCLK and 32K synchronizing problem causes clock-gating error

Impact:

Due to clock-gating error interrupt based on 32K clock does not trigger. Interrupt could not be generated in SLEEP mode if register configuration does not follow some rules.

Description:

When HFCLK and 32K clock are available to the system and both are active, then 32K is synchronized to HFCLKIN.

The state of HFCLKIN depends on CLKEN. If CLKEN is low then HFCLKIN is in OFF state. In this situation, if HFCLKOUT is configured to keep HFCLKOUT active then the internal clock synchronization does not function correctly and the 32K buffer clock is stuck. This does not allow any interrupt based on 32K to be triggered (for example, keypad and GPIO).

Workaround:

If CLKEN is configured low for power consumption, then HFCLKOUT must not be configured to keep HFCLKOUT active. The recommended configurations for CLKEN and HFCLKOUT are:

- CLKEN assigned to all three device-groups
- HFCLKOUT assigned to P3 only, and remap sleep state to off

26 VDD1, VDD2, may have glitches when their output value is updated

Impact:

The OMAP device may reboot if the VDD1 or VDD2 go below the core minimum operating voltage.

Description:

Negative glitches may occur on VDD1, VDD2 output. It occurs when the output voltage is changed and the DCDC are running on their internal oscillator.

Workaround:

- If fail rate is acceptable, leave application like this.
- Partial software fix is available (For more information, see Glitch_Sleep_Settings.pdf.).
- Final fix will be available in next silicon revision (Hardware fix)

27 VDD1 and / or VDD2 DCDC clock may stop working when internal clock is switched

from internal to external

Impact:

VDD1 and/or VDD2 output voltages may collapse if clock stops.

Description:

VDD1 and/or VDD2 clock system may hang during switching the clock source from internal oscillator to external. In such situation, DCDC outputs collapse. The feature is enabled by asserting bit EXT_FS_CLK_EN of registers VIO_OSC, VDD1_OSC and VDD2_OSC to '1'.

Workaround:

1. Recommendation is not to use DCDC external clock synchronization feature.
2. This will be deactivated for next silicon revision.

28 VIO efficiency loss when VBAT is less than 3.0V and the DCDC is in PFM mode

Impact:

VIO power consumption slightly increases, versus the expected value, when device is in SLEEP mode.

Description:

In PFM mode DCDC is running continuously instead of toggling by burst. This phenomenon occurs for battery voltage below 3V. It is strongly linked with the board parasitic.

Workaround:

Software work around:

- Remap VIO to run in "ACTIVE" during the "SLEEP" periods.
- Configure the VIO DCDC according to the "Configuring TPS65950 DCDC in PFM for low VBAT" application note.

For more information, see Configuring_TPS65950_DCDC_in_PFM_for_low_VBAT.pdf

29 GROUP2 resource settings result in unexpected behavior (applicable only for TPS65920/30 devices)

Impact:

Resources associated with GROUP2 may not have the expected functionality.

Description:

An internal control signal controlling the states of resources associated to GROUP2 is erroneously tied to GND. If a power resource is associated to GROUP2 then it will transition to SLEEP state if the corresponding LVL_WAKEUP for GROUP2 is set to '1'.

Workaround:

Do not set any power resource to GROUP2. This can be done in software. Please refer to the DEV_GRP_<Resource_Name> register.

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