TPS65950 Real-Time Clock Timing Compensation

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ABSTRACT

This application note provides information about how to use the TPS65950 device real-time clock (RTC) timing compensation mechanism. It begins with an overview of why compensation is desirable and how it is implemented in the TPS65950. Later sections of the document describe how the feature is implemented by interfacing to externally provided capabilities. A systems overview, supported by representative calculations, is also provided.

1 TPS65950 RTC Timing Compensation Overview

1.1 32-kHz Clock Terminology

For the purposes of this document, an oscillator is the same thing as a clock (see , *Clocks*, in the TPS65950 TRM [SWCU050B]).

As is common practice, the term 32 kHz refers to a frequency of 32.768 kHz, which is a convenient frequency for timekeeping because a signal at 32.768 kHz can be divided by a 15-stage counter to derive 1-second timing. Although a 32-kHz clock has a nominal frequency of 32.768 kHz, the exact frequency can be anywhere in the frequency tolerance range of a crystal (100 ppm is the least accurate). When a clock signal is precisely on 32.768 kHz, the signal name is modified (for example, "exact") to indicate the precision.

1.2 Advantage of Compensation

The TPS65950 RTC contains a compensation mechanism that provides a way to maintain high long-term timekeeping accuracy even when the 32-kHz signal (the RTC timebase) is at the limit of its design tolerance. With a 100-ppm tolerance 32.768-kHz crystal at design limits, the RTC error after 30 days is 4 minutes and 19 seconds. The compensation mechanism can typically reduce this error to less than 30 milliseconds (an improvement by a factor of more than 9000).

Thus, the compensation mechanism maintains accuracy in the 32-kHz oscillator. In the compensation procedure, the external processor calculates the drift of the 32-kHz oscillator and then loads the compensation registers (RTC_COMP_LSB_REG and RTC_COMP_MSB_REG) with the drift compensation value calculated during the measurement. If the RTC_CTRL_REG register AUTO_COMP_EN bit is enabled, the value of COMP_REG (in twos complement) is added to the RTC 32-kHz counter each hour and 1 second. When COMP_REG is added to the RTC 32-kHz counter, the duration of the current second becomes [(32768-COMP_REG)/32768] seconds; therefore, it is possible to compensate the RTC with 1/32,768-second time unit accuracy each hour.

These steps outline the required calibration process. This discussion does not include details about the requirement to provide an accurate external frequency reference and suitable software on the external processor to perform the calibration. Table 1 maps the distribution of responsibilities between the RTC and the external processor for drift compensation.

Table 1. Task Distribution Between External Processor and RTC for Drift Compensation

External Processor	RTC
Measure the 32-kHz oscillator drift.	
Calculate the drift compensation for 1 hour.	
	Every hour, drift compensation value is added to the RTC 32-kHz counter.

2 RTC Compensation Process

RTC compensation has two components:

- Circuitry internal to the TPS65950
- Circuitry and calculations external to the TPS65950

2.1 Inside the TPS65950

The RTC functions by counting the 32-kHz clock. For each hour there are fixed-length seconds and one variable-length second.

2.1.1 Fixed-Length Seconds

There are 3599 fixed-length seconds. Each second is exactly 32,768 ticks of the 32-kHz clock (see Figure 1). Thus, if the clock is precisely on frequency, each fixed-length second is exactly 1 second long.

2.1.2 Variable-Length Second

The variable-length second is the method by which RTC compensation works. There is 1 variable-length second for each hour in the RTC.

Instead of always being 32,768 ticks of the 32-kHz clock (like fixed-length seconds), the length (duration) of a variable-length second can be changed between a maximum and a minimum amount (see Figure 1) .

The length (duration) of the variable-length second is related to ticks of the 32-kHz clock by the equation:

ticks = (32,768 – RTC_COMP)

RTC_COMP is the time-correction coefficient and the concatenation of the values in two 8-bit TPS65950 registers: RTC_COMP_LSB_REG and RTC_COMP_MSB_REG. RTC_COMP can vary between –32,768 and +32,767.

If RTC_COMP is at its maximum positive value of +32,767, the variable-length second is (32,768–32,767) = 1 tick of the 32-kHz clock. If the 32-kHz clock is precisely on frequency, that is 30.518 µsec, so the length (duration) of the variable-length second can be decreased to almost 0.

If RTC_COMP is at its maximum negative value of –32,768, the variable-length second is (32,768–(–32,768) = 65,536 ticks of the 32-kHz clock. If the 32-kHz clock is precisely on frequency, that is 2 seconds, so the variable-length second can be twice as long as a true 1-second length.

By changing the time-correction coefficient (RTC_COMP), the variable-length second can insert or remove (~) up to 1 second in every hour of the RTC with a step size of roughly 30.5 µsec (the duration of the variable-length second can be adjusted in 1-tick steps of the 32-kHz clock). That is how the variable-length second can be used to maintain high long-term timekeeping accuracy of the RTC, even when the 32-kHz oscillator (the RTC timebase) is not precisely on frequency.

Figure 1 shows how RTC timing repeats each hour.

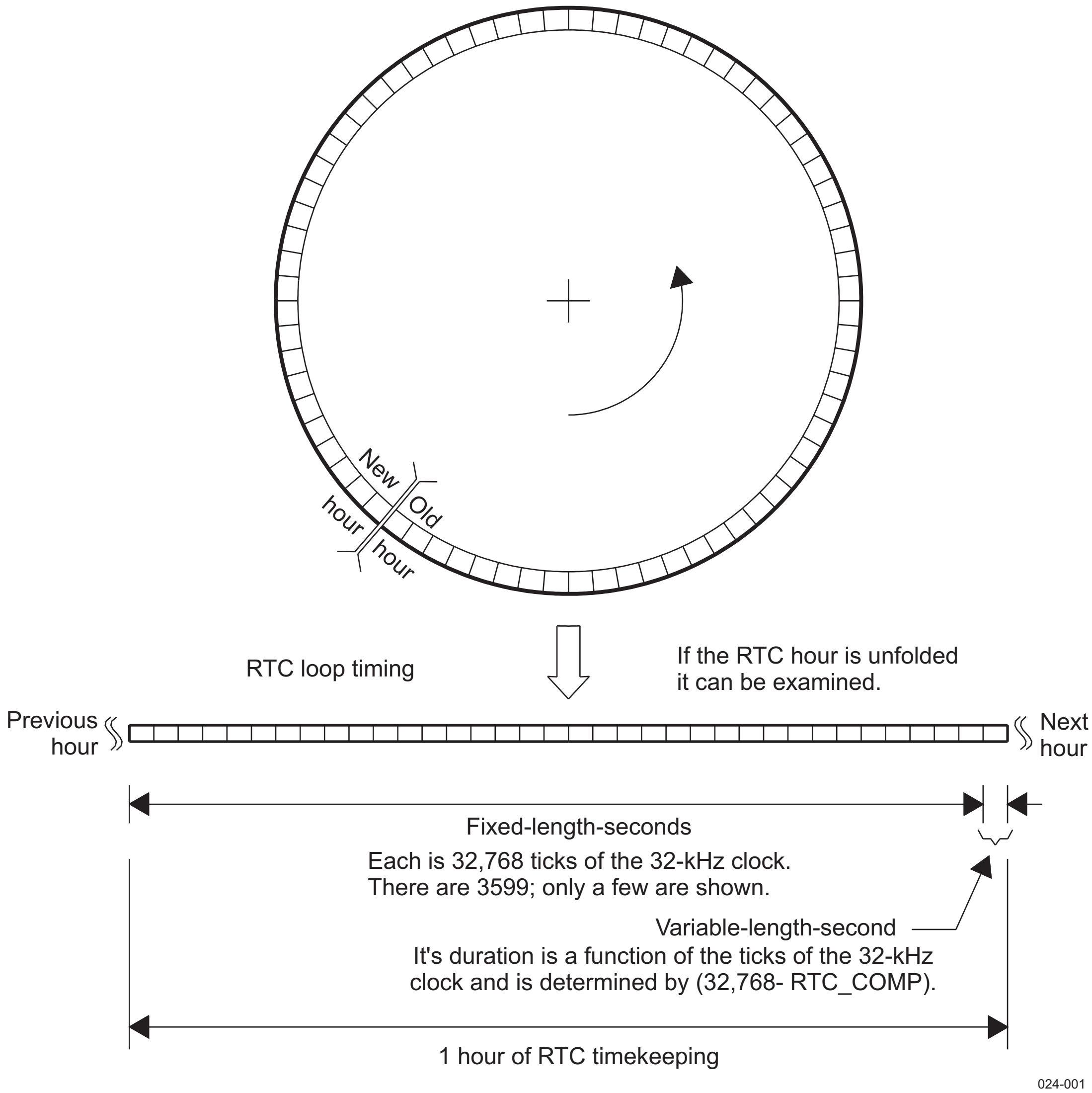

Figure 1. RTC Timing

2.2 Outside the TPS65950

The mechanism for determining the required time correction coefficient (RTC_COMP) must be provided externally.

There must be an external comparison of the 32-kHz clock to a high-frequency source of great frequency accuracy. From that comparison comes an error signal that is used to calculate the time correction coefficient required to reduce the per-hour timekeeping deviation of the RTC to near 0.

2.2.1 Sample Design Model

For this document, a particular design has been implemented as a model. Other methods may be equally valid, depending on the situation.

To measure the frequency of the 32-kHz clock (so that the required time correction coefficient for the RTC can be calculated), the frequency is compared to an available high-frequency clock, such as 19.2, 26.0, or 38.4 MHz; these are the frequencies used by the TPS65950 for its HF_CLK, so one will be available.

The 32-kHz clock gates a measurement of the high-frequency clock for a sample period and the number of cycles of the high-frequency clock that are counted (counts) during the sample period is noted (see Figure 2).

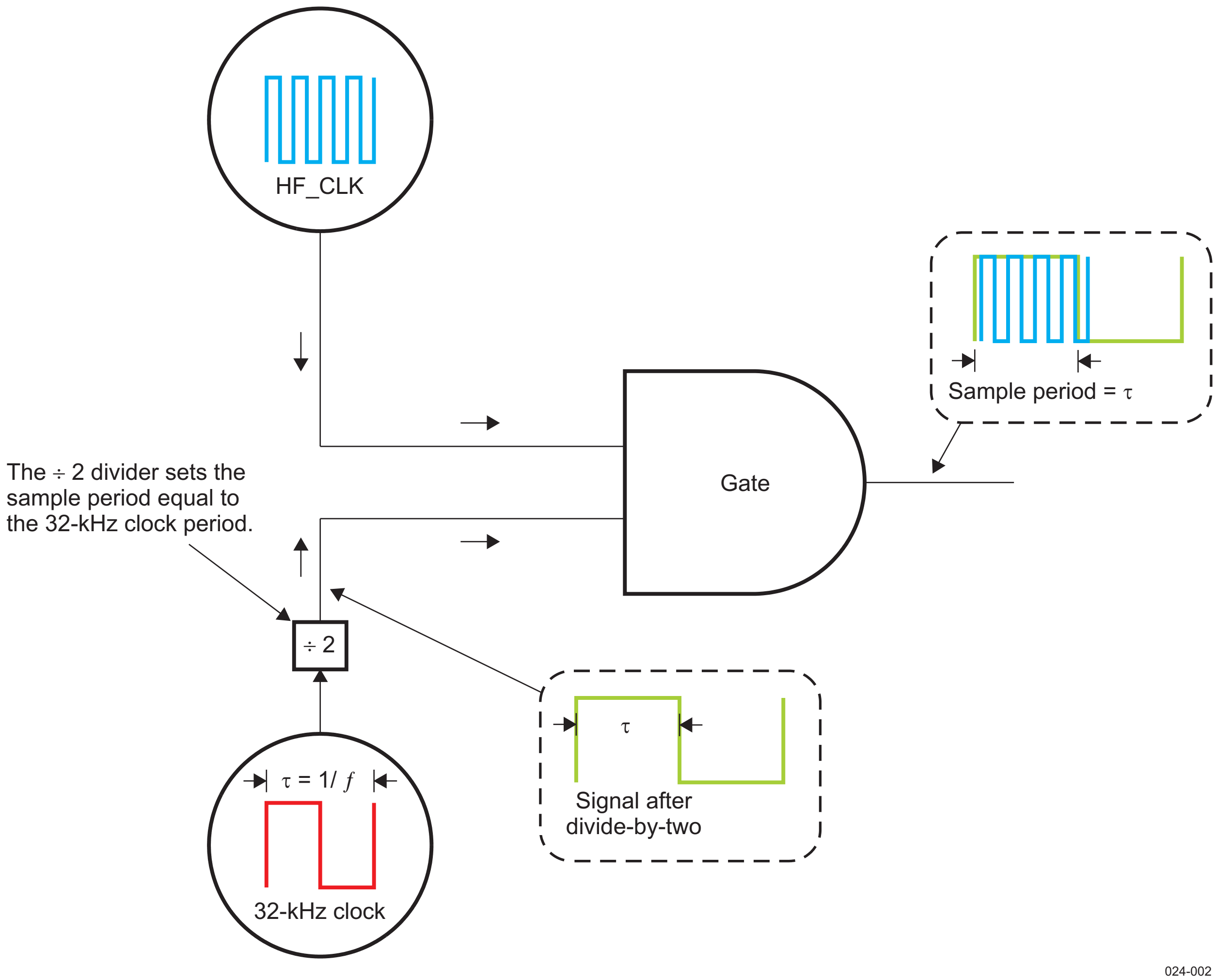

Figure 2. Sample Clock Comparator Block Diagram

If the 32-kHz clock and the high-frequency clock are exactly on frequency, and the length of the sampling period (based on the 32-kHz clock) is correct, the number of cycles of the high-frequency clock is known to occur during the sampling period (with one potential source for error described in the next paragraph). A difference between the calculated counts and the actual counts measured is an error signal resulting from a variation in the sampling time caused by the 32-kHz clock being off frequency. This error signal generates the time correction coefficient required to reduce the RTC timekeeping error to an extremely low value (typically a few 10s of ms during a month).

An error in the count of the high-frequency clock can be caused by nonsynchronicity of the high-frequency clock and the 32 kHz clock:

- When the sample period turns on, it is not possible to tell during which portion of the high-frequency signal the turn-on transition occurs.
- When the sample period turns off, it is not possible to tell during which portion of the high-frequency signal the turn-off transition occurs.

As a result of these uncertainties, almost two counts of the high-frequency signal can be lost. To minimize this effect, the duration of the counting period (based on the 32-kHz clock) must last long enough for the number of counts (transitions) of the high-frequency clock to be much greater than the two (possibly) missing counts (transitions).

This is accomplished by using a lower-frequency gating clock than shown in Figure 2. Instead of using the 32-kHz clock to directly control the measurement duration, a lower-frequency (longer period) signal derived from the 32-kHz clock can be used; this has the same effect as counting the high-frequency clock for more than just one 32-kHz period.

If the 32-kHz clock directly gates the sampling of the high-frequency clock (as shown in Figure 2 with the divider setting the sample period to equal the period of the 32-kHz signal):

$$\text{Equation 1: Sample period} = \tau_{(32kHzCLK)} = (1/f_{(32kHzCLK)}) \approx 30.5\ \mu S$$

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If the high-frequency clock being sampled is 26 MHz:

$$\text{Equation 2: Counts}_{(HFCLK)} = [(f_{(HFCLK)})/\tau_{(32kHz)}] \approx 793$$

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Even if the 32-kHz clock is exactly at 32.768 kHz, there is the potential for an error of ~2 (out of 793 calculated) counts of the 26-MHz signal.

3 Formula Deviations and Comments

3.1 The Error Signal and Frequency of the 32-kHz Clock

The error signal is the difference between the actual number of counts of the high-frequency clock during the measurement period (based on the duration of the actual 32-kHz clock) and the number of counts calculated based on the duration of an exact 32-kHz clock.

Note: Missed counts, as discussed in Section 2.2.1, *Clock Comparator Considerations*, cannot be calculated.

Error signal = (actual counts) – (exact counts)

Where:

- (actual counts) = counts of the HF clock with actual 32-kHz clock
- (exact counts) = counts of the HF clock with exact 32-kHz clock

Even though missed counts cannot be calculated, their effect can be minimized by increasing the sampling period to greater than that defined by one period of the 32-kHz clock.

Let m = multiplier of the sampling period set by a single oscillation of the 32-kHz clock.

Then count (actual) =

$$\text{Equation 3a: Count (actual)} = (f_{(HF\_CLK)}/f_{(32kHz\_actual)}) * m$$

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And count (exact) =

$$\text{Equation 3b: Count (exact)} = (f_{(HF\_CLK)}/f_{(32kHz\_exact)}) * m$$

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Then the error signal =

$$\begin{aligned}\text{Equation 3c: Error signal} &= ((f_{(HF\_CLK)}/f_{(32kHz\_actual)}) * m) - ((f_{(HF\_CLK)}/f_{(32kHz\_exact)}) * m)\\ &= m * ((f_{(HF\_CLK)}/f_{(32kHz\_actual)}) - (f_{(HF\_CLK)}/f_{(32kHz\_exact)}))\end{aligned}$$

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Solving for the frequency of the 32-kHz clock yields:

$$\text{Equation 4: } f_{(32kHz\_actual)} = m \frac{f_{(HF\_CLK)}}{\left[\text{Error signal} + m \frac{f_{(HF\_CLK)}}{f_{(32\_kHz\_exact)}}\right]}$$

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3.2 RTC Timekeeping Loop

As described in Section 2, *RTC Compensation Process*, the ability of the RTC to maintain high accuracy over an extended period is made possible by the variable-length second that occurs once an hour; it can increase or decrease the length of time it takes the RTC to complete an hour's timekeeping by ± 1 second.

If the frequency of the 32-kHz crystal is slightly too low (its period is longer than required for precise timing accuracy so the fixed-length seconds take longer to complete), the variable-length second is made slightly shorter than 1 second so that the overall RTC period is correct.

If the frequency of the 32-kHz crystal is slightly too high (its period is shorter than required for precise timing accuracy so the fixed-length seconds complete too quickly), the variable-length second is made slightly longer than 1 second so that the overall RTC period is correct.

While a fixed-length second always consists of 32,768 ticks of the 32-kHz clock, the variable-length second can be changed in duration by having it consist of n ticks of the 32-kHz clock defined by:

$$\text{Equation 5a: Variable-length second clock ticks} = (32{,}768 - RTC\_COMP)$$

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The duration (length) of the variable-length second is found by multiplying the number of ticks times the length of each tick:

$$\text{Equation 5b: Variable-length second duration} = (32{,}768 - RTC\_COMP) * (1/f_{(32\_kHz\_actual)})$$

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The duration (length) of the 3599 (in each hour of RTC timekeeping) fixed-length seconds is found by multiplying the number of ticks per RTC second (always 32,768 for fixed-length seconds) times the length of each tick times the number of fixed-length seconds in an hour (3599):

$$\text{Equation 6: Fixed-length sections duration (each hour)} = 32{,}768 * (1/f_{(32\_kHz\_actual)}) * 3599$$

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The total time taken by the RTC loop timing (recurring each hour) is the sum of the variable-length second duration and the fixed-length seconds duration:

$$\text{Equation 7: RTC loop timing (seconds)} = [(32{,}768 - RTC\_COMP)/(f_{(32\_kHz\_actual)})] + [(32{,}768 * 3599)/(f_{(32\_kHz\_actual)})]$$

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3.3 Solving for the RTC Timekeeping Correction Coefficient (RTC_COMP)

To solve for RTC_COMP, the RTC loop timing (see Section 3.2, *RTC Timekeeping Loop*) is set to equal 3600 (the number of seconds in 1 hour):

$$\text{Equation 8a: } 3600 = [(32{,}768 - RTC\_COMP)/(f_{(32\_kHz\_actual)})] + [(32{,}768 * 3599)/(f_{(32\_kHz\_actual)})]$$

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and the equation is solved for RTC_COMP:

$$\text{Equation 8b: } RTC\_COMP = 3600 * (32{,}768 - f_{(32\_kHz\_actual)})$$

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4 Conclusion

This document described the following topics:

- TPS65950 RTC timing compensation: How compensation of the TPS65950 helps achieve long-term timing accuracy
- The RTC compensation process:

  - Inside the TPS65950: The compensation coefficient (RTC_COMP) capability provided in the RTC circuitry and its working
  - Outside the TPS65950: A representative clock comparator circuit and its working and limitations
- Formula derivations:
  - 32 kHz-clock frequency (Equation 4)
  - RTC loop timing (Equation 7)
  - RTC timekeeping coefficient (Equation 8b)

Appendix A Glossary and References

A.1 Commonly Used Terms and Expressions

COMP_REG	Same as RTC_COMP. The original design specification used this term when describing the compensation formula.
Fixed-length seconds	The 3599 periods in the RTC operation each hour during which the number of 32-kHz clock source ticks counted is fixed at 32,768 for each period. Each fixed-length second is nominally 1 second long and any variance is proportional to the ratio of the actual 32-kHz clock frequency and 32.768 kHz. Each hour counted by the RTC is composed of the 3599 fixed-length seconds and 1 variable-length second. Fixed-length seconds are invariable and do not play a role in the RTC time correction mechanism.
RTC loop timing	The length of time required for the RTC to complete 1 hour. Any deviation in RTC loop timing from precisely 1 hour is a function of the frequency of the 32-kHz clock and the value of the time correction coefficient.
Tick	One cycle (Hz) of the 32.768-kHz clock source (controlled directly by a quartz crystal or supplied from an external source)
Time correction coefficient (RTC_COMP)	Variable used to set the length (duration) of the variable (RTC_COMP)-length second used by the RTC timekeeping correction mechanism. The time correction coefficient is also known as RTC_COMP (RTC compensation) when referring to its derivation from the concatenation of the values in two TPS65950 registers (RTC_COMP_LSB_REG and RTC_COMP_MSB_REG). RTC_COMP can have a value between –32768 and +32767. RTC_COMP is also known as COMP_REG in reference to the compensation formula.
Variable-length second	The period in RTC operation each hour during which the number of 32-kHz clock ticks counted is not fixed for the duration of the period but instead can be varied by activating and using RTC_COMP. By changing RTC_COMP between its maximum positive and negative limits, the length of the variable-length-second can be changed from (essentially) 0 and 2 seconds. Each hour counted by the RTC is composed of 1 variable-length second and 3599 fixed-length seconds. The variable-length second is the method by which long-term high-accuracy timekeeping can be achieved by the RTC even when frequency tolerance of the 32-kHz timebase is at its limit.

A.2 References

- TPS65950 Technical Reference Manual (SWCU050A)
- TPS65950 Data Manual (SWCS032)

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