APPLICATION NOTE

SKY77529 Rx-Tx Front-End Module – Implementation

Applicability: SKY77529 Tx Front-End Module for Dual-Band GSM / GPRS / EDGE

Introduction

The SKY77529 Front End Module (FEM) supports dual-mode, quad-band power amplification and antenna path switching for GMSK / EDGE applications in systems using a specific direct-launch EDGE architecture. The antenna switch provides 4 linear ports for WCDMA pass-through. Integrated power detection is supported through RF linear power detection. Signal path switching is supported with an integrated SP8T switch. ESD protection and DC blocking of the switch are also integrated. Device control is accomplished with a Serial Peripheral Interface (SPI) bus function. All information for configuring mode, band, and enable are controlled through a bidirectional three wire serial bus control interface.

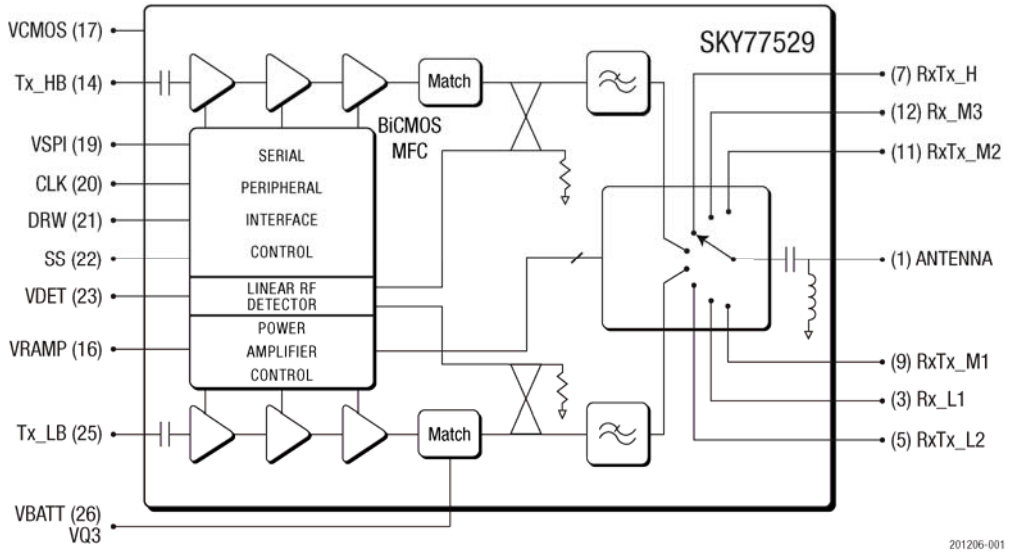

Figure 1. SKY77529 Functional Block Diagram

SKY77529 Power Amplifier Control Overview

The power amplifier supports a constant gain, linear operation for EDGE mode and a saturated operation for GMSK mode. Figure 2 depicts the bias control architecture for the SKY77529.

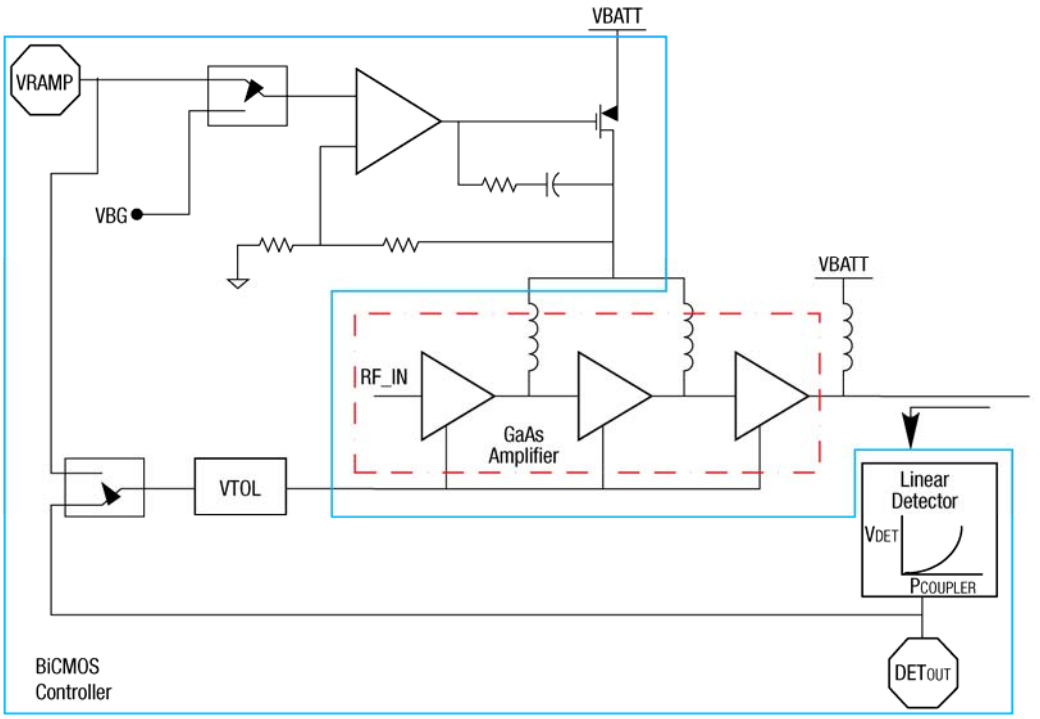

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Figure 2. Bias Control Architecture – SKY77529

During the linear EDGE operation, amplifier quiescent current is maintained constant, independent of temperature, to maintain constant intercept performance. The RF input drive level of the amplifier controls output power; the VRAMP signal provides analog control of the bias points. Output power is detected and translated to DC voltage via a linear detector circuit and buffer amplifier. DC output of the RF detector is linearly related to output power.

During saturated GMSK operation, the RF input drive is held constant while saturation characteristics of the amplifier are used to control output power. Stage 1 and stage 2 amplifiers are forced into saturated mode by reducing the collector voltage to limit the large signal gain of the driver stages, reducing the input level to the final stage amplifier. Coincident reduction of quiescent current in the amplifier reduces the small signal gain and current drain.

Closed loop power control is provided external to the controller. In the Application Diagram (Figure 3), the transceiver forms a closed loop with the SKY77529. During EDGE mode, the transceiver monitors the linear detector output voltage and modifies the RF input during the burst ramp. VRAMP is used to set the bias point of the amplifier stages. During GMSK mode, the detector is monitored while VRAMP is used to set output power. VDET is also used internally to set the bias points of the amplifier stages.

The Application Diagram (Figure 3) indicates the recommended passive components external to the FEM. These include components for power supply filtering, control signal filtering, input matching, and ESD protection. The values for the VCC bypass capacitors are dependant on the noise level on the phone board.

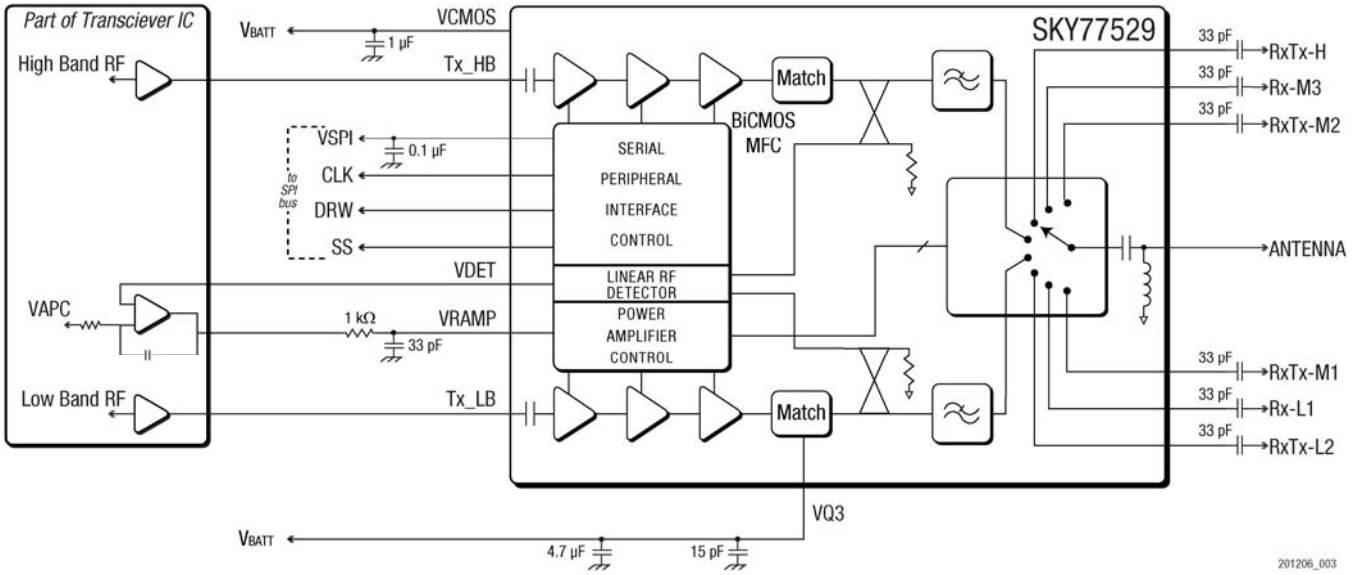


Figure 3. SKY77529 Application Diagram

VRAMP Filter

It is advisable to use a first order RC network on the VRAMP line to filter noise introduced by the baseband DAC. The filter should be so designed to avoid slowing down the power mask timing requirements.

Note: Recommended RC network values: 1 kΩ resistor with a 33 pF capacitor.

VRAMP Profile for GMSK Operation

All ramping properties are determined by and limited by the specific baseband device and control software.

Antenna Port ESD Network

An LC network external to the Antenna is required to meet the IEC 61000-4-2 standard.

Rx Port DC Block

The DC offset of up to 400 mV on the Rx ports can be blocked with the 33 pF series elements.

Logic and Input Settings

Table 1. Recommended VRAMP Bias EDGE Mode (8PSK, High Band, Low Band)

POUT (dBm)	27.8	27.0	26.0	25.0	24.0	23.0	22.0	21.0	20.0	<20.0
VRAMP (V) at low band	1.2	1.1	1.0	0.8	0.7	0.6	0.6	0.6	0.5	0.5
VRAMP (V) at high band		1.4	1.3	1.1	1.0	0.9	0.8	0.7	0.6	0.5

SKY77529 PHONE BOARD APPLICATION CIRCUIT

Layout Guidelines for Battery Bypassing

Phone board layout is a complex issue and one key area is supply decoupling. Figure 4 shows the transient current for VBATT will be supported by the nearby capacitance. The VBATT line of the FEM requires low frequency bypassing capacitance. In modern communication systems, a GSM PA draws rapid pulses of current that can cause a significant transient during the transmission. This might affect the output power mask at high power levels. Most lab supplies are not suited for digital communications and do not emulate the phone board battery condition. Hence, in some cases a higher value capacitor of 68 µF may be required.

Routing the VBATT trace on the phone board layout, it is critical to direct the primary line to VQ3 (pad 26), and a secondary line to VCMOS (pad 17). This assures proper operation of the current limit function of the FEM and avoids excessive voltage drop to the PA output stage.

On the phone board, battery ESR will reduce the transient voltage pulse and should not require more than a 4.7 µF bypass capacitor. This bypass capacitor should be a good quality ceramic or tantalum capacitor.

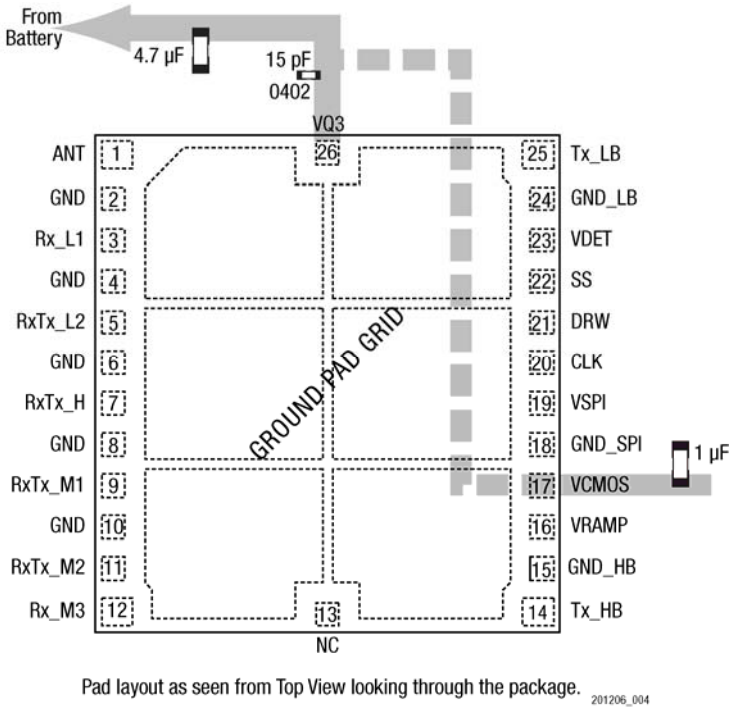


Figure 4. Application Circuit Layout Diagram for SKY77529 Front-End Module

SPI Interface Control

The SKY77529 supports a bidirectional three-wire serial bus control interface. All information for configuring mode, band, and enable are controlled through this bus. Read-back functionality exists within the SPI interface to evaluate device type and status information.

Three main registers exist within the SPI interface. These registers include the Device Address register which is hardwired to identify the device type and vendor; the Configuration register which is the Write register containing the control information; and the Status register which is the Read register that controls device status information. Table 1 details these register mappings. The core logic of the SPI functions at the battery voltage eliminating the need for level translation between the configuration and status register. Level translation from the VSPI reference up to the battery voltage is included within each of the digital interface pads. The SPI data pad supports bidirectional operation and includes an output driver. The output enable (SPI_OEN) signal generated within the SPI control block is active low.

Table 2. SPI and Logic Interface

Spec	Minimum	Typical	Maximum	Unit	Notes
Battery Voltage	2.9	3.5	4.8	V	Battery
VSPI voltage ref	1.5		2.86	V	
Clock Frequency			26	MHz	
Core interface voltage	2.7	3.5	4.8	V	Battery voltage
VSPI logic low	0		0.5	V	
VSPI current			1	mA	
Pad logic high input	0.7*V(VSPI)		V(VSPI)	V	
Pad logic low input	0		0.3*V(VSPI)	V	
Pad logic input R	100			kΩ	
Pad logic input cap			2	pF	
SPI Data out Low	0		0.2*V(VSPI)	V	
SPI Data out High	0.8*V(VSPI)		V(VSPI)	V	
SPI Data load			24	pF	

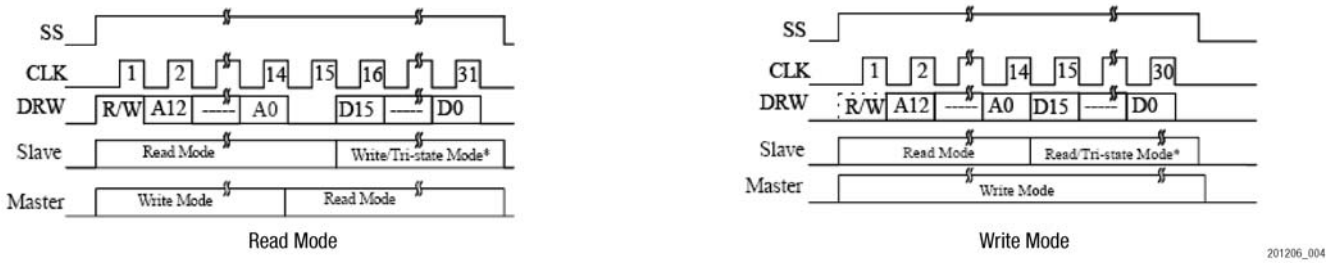


Figure 5. Read / Write

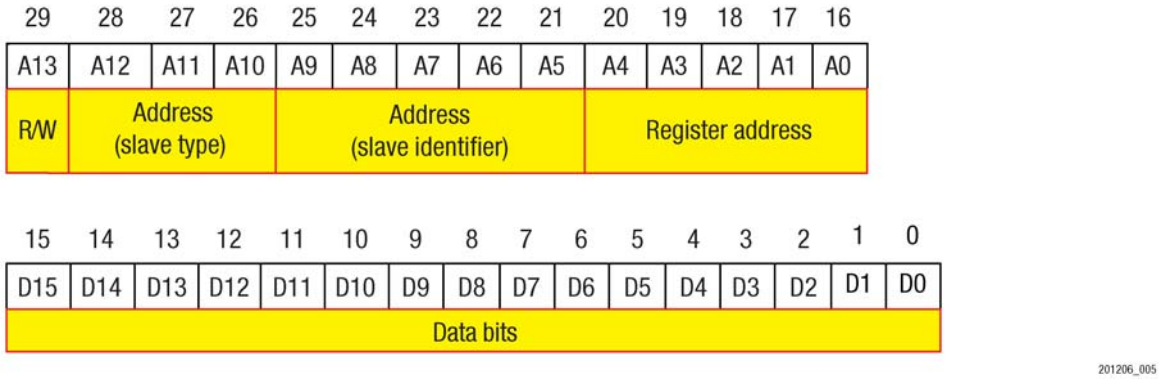


Figure 6. SPI Telegram with Address and Data Field

Table 3. SKY77529 SPI Address Bit Mapping

Bit	Description	Default	Notes
A13	Read / Write	0	Read = 0, Write = 1
A12	Slave device Type MSB	0	Slave PA device = 000
A11	Slave device type	0	Slave PA device = 000
A10	Slave device type LSB	0	Slave PA device = 000
A9	Slave device ID MSB	0	Slave SWKS device = 00100
A8	Slave device ID	0	Slave SWKS device = 00100
A7	Slave device ID	1	Slave SWKS device = 00100
A6	Slave device ID	0	Slave SWKS device = 00100
A5	Slave device ID LSB	0	Slave SWKS device = 00100
A4	Register Address MSB	0	Slave SWKS device = 00100
A3	Register Address	0	Slave SWKS device = 00100
A2	Register Address	0	Slave SWKS device = 00100
A1	Register Address	0	Slave SWKS device = 00100
A0	Register Address LSB	0	Read = 0, Write = 1

Table 4. SKY77529 SPI Bus Mapping

bit	Write	Read	Default Write
D15	FE Boost Converter on/off can be switched on/off independent of selected path	Reserved (default 0)	0
D14	FE select 4	Reserved (default 0)	0
D13	FE select 3	Reserved (default 0)	0
D12	FE select 2	Reserved (default 0)	0
D11	FE select 1	Reserved (default 0)	0
D10	Sensor configuration	Reserved (default 0)	0
D9	Sensor configuration	Current Sensor feedback	0
D8	Reserved (default 0)	Reserved (default 0)	0
D7	Reserved (default 0)	Reserved (default 0)	0
D6	Reserved (default 0)	Reserved (default 0)	0
D5	Current Sensor Current inflection point	Reserved (default 0)	1
D4	Current Sensor Current inflection point	PA temperature > Threshold 1	0
D3	Current Sensor Current inflection point	PA temperature > Threshold 2	0
D2	Tx Enable Switch on/off PA Engine and detector	Reserved (default 0)	0
D1	PA Mode selection 8PSK / GMSK	Reserved (default 0)	0
D0	PA Mode selection Low band / High band	Reserved (default 0)	0

Table 5. PA Temperature (Rear Register)

D4	D3	PA Temperature Sensor
0	0	T < T1 °C
0	1	T > T1 °C
1	0	Not used
1	1	T > T2 °C
0	0	Not used
0	1	Not used
1	0	Not used
1	1	Not used

Table 6. Current Sensor Flag (Read Register)

D11	D10	D9	Current Sensor Feedback
0	0	0	Sensor not active
0	0	1	Sensor active
0	1	0	Not used
0	1	1	Not used
1	0	0	Not used
1	0	1	Not used
1	1	0	Not used
1	1	1	Not used

Table 7. SPI Write Programming Truth Table

D0	Band Select				D10	D9	Sensor Configuration		
0	Low band				0	0	Current sensor FB Off		
1	High band				0	1	Current sensor FB Off		
D1	Mode Select				1	0	Current sensor FB On		
0	GMSK				1	1	Current sensor FB On		
1	8PSK								
D2	Tx Enable				D15	FE Boost Converter			
0	PA Off				0	Off			
1	PA On				1	On			
			Current Sensor						
D5	D4	D3	Mode = GMSDK	Mode = 8PSK	D14	D13	D12	D11	FE Status
0	0	0	1.6 A	0.6 A	0	0	0	0	Off
0	0	1	1.7 A	0.7 A	0	0	0	1	Tx_M GMSK ANT
0	1	0	1.8 A	0.8 A	0	0	1	0	Tx_L GMSK ANT
0	1	1	1.9 A	0.9 A	0	0	1	1	Reserved
1	0	0	2.0 A	1.0 A	0	1	0	0	Rx_L1
1	0	1	2.1 A	1.1 A	0	1	0	1	RxTx_M2
1	1	0	2.2 A	1.2 A	0	1	1	0	Rx_M3
1	1	1	2.3 A	1.3 A	0	1	1	1	Reserved
D8	D7	D6	Not Assigned to Specific Function		1	0	0	0	Rx/Tx_L2
0	0	0	Default		1	0	0	1	Rx/Tx_M1
0	0	1			1	0	1	0	Rx/Tx_H
0	1	0			1	0	1	1	Reserved
0	1	1			1	1	0	0	Reserved
1	1	0			1	1	1	1	Reserved
1	1	1							

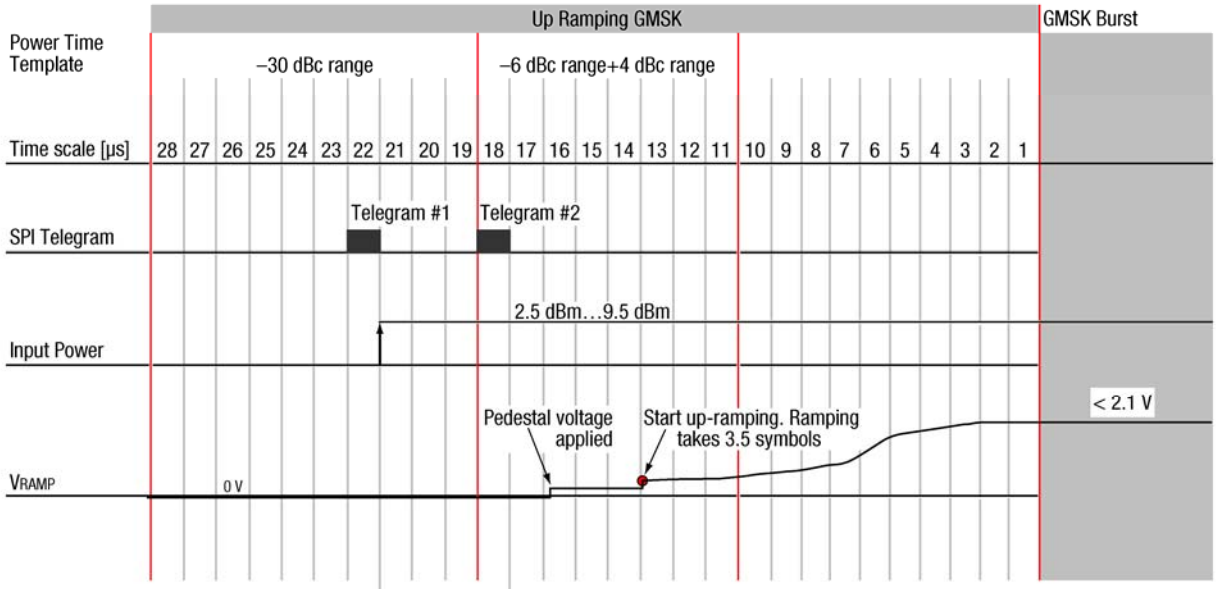
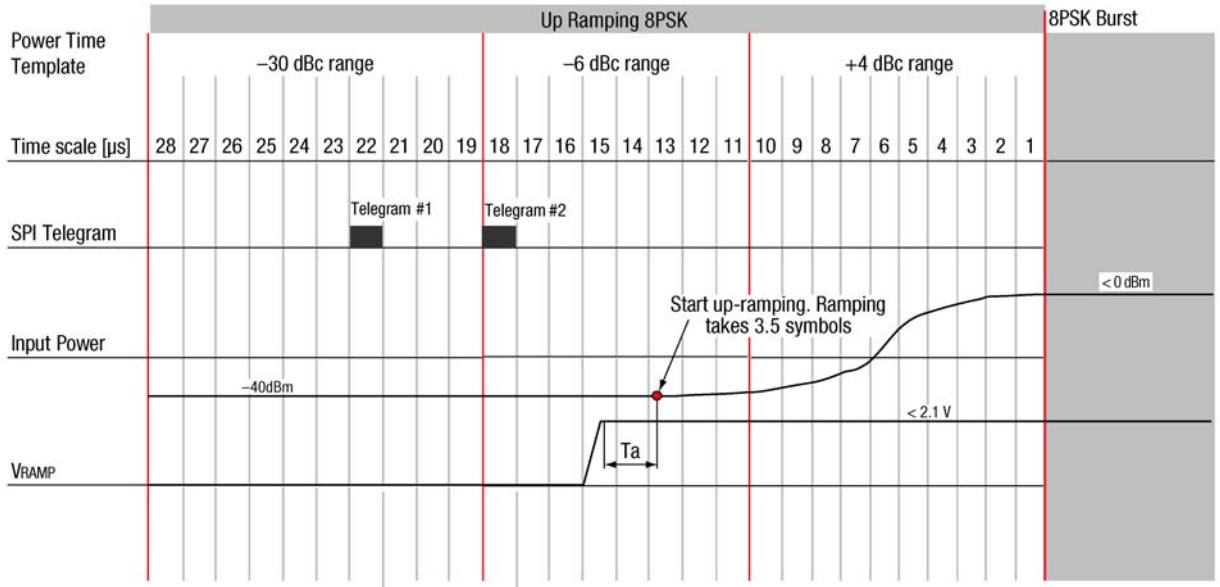


Figure 7. Timing Diagram – Up Ramping GMSK



		Telegram #1	Telegram #2
D15	Boost Converter	0	1
D14	FE select 4	1	0
D13	FE select 3	0	0
D12	FE select 2	1	1
D11	FE select 1	0	0
D10	Sensor config	0	1
D9	Sensor config	0	0
D8	reserved	0	0
D7	reserved	0	0
D6	reserved	0	0
D5	Current sensor	0	0
D4	Current sensor	0	1
D3	Current sensor	0	1
D2	Tx Enable	1	1
D1	PA Mode	0	0
D0	PA Band	0	0

Example: GMSK, 900 MHz, current threshold = 1.9 A

Note:
Telegram #1
- Enables the PA
- Selects the right band
- PA mode is always GMSK (also in 8PSK case)
- RXTXpath selected to meet isolation

Telegram #2
- Enables the switch and selects the right path
- Current threshold is set; sensor is configured
- Selects the correct mode

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Figure 8. Timing Diagram – Up Ramping 8PSK

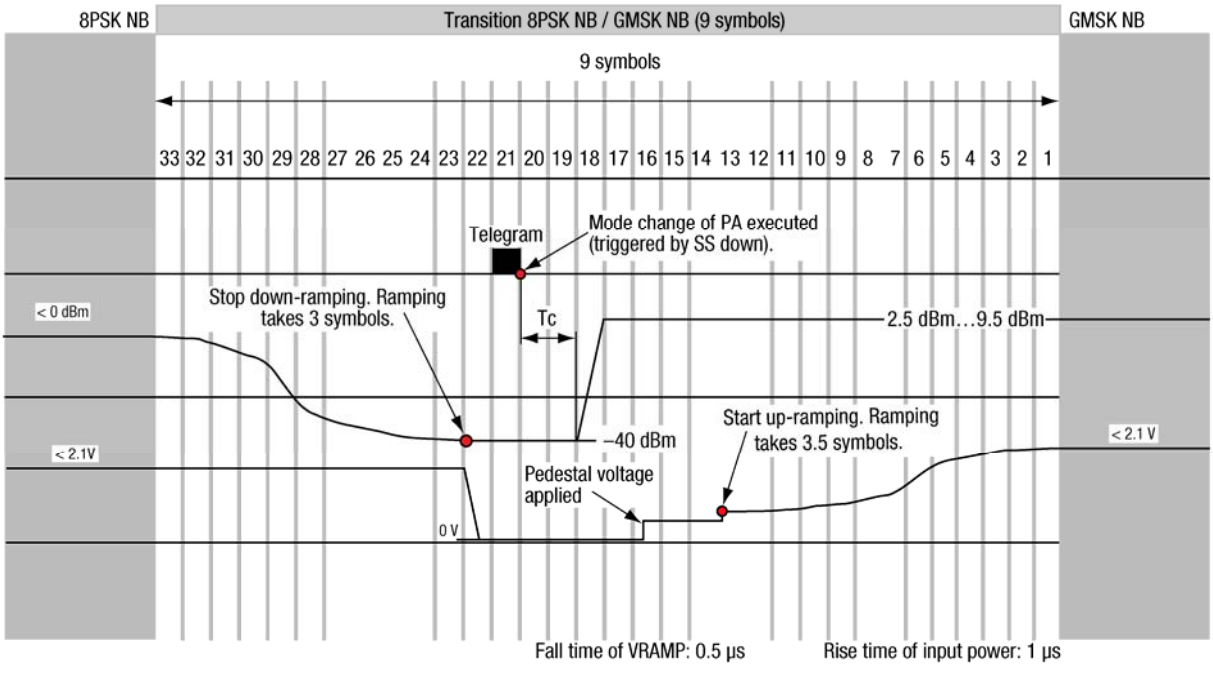

Figure 9. Timing Diagram – Transition 8PSK NB to GMSK NB

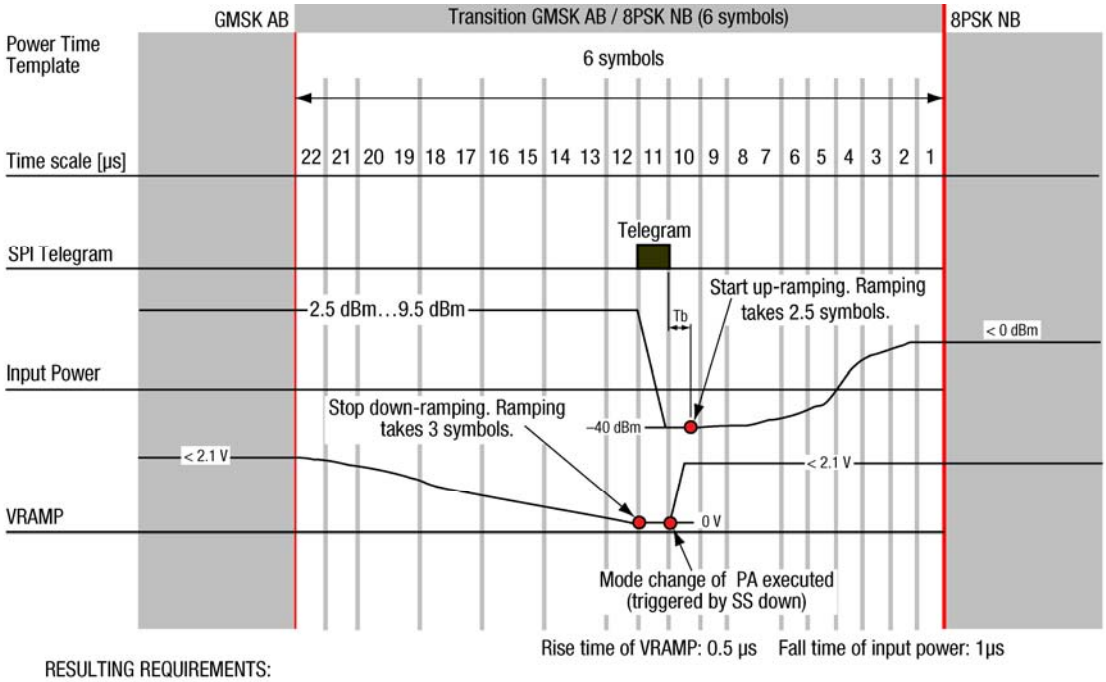

Figure 10. Timing Diagram – Transition GMSK AB to 8PSK NB

Linear Detector

Power detection is supported through an integrated linear detector. The module level interface between the power amplifier outputs and detector inputs is accomplished with two directional couplers integrated onto the MCM laminate. Figure 11 is a block diagram of the SKY77529 detector/coupler; Figure 12 is a block diagram of the linear detector. The coupler outputs are routed to the controller IC. Separate bond wires connect the HB and LB signals to their respective detector inputs. The controller's logic decoder enables the appropriate detector during the TX burst (i.e. HB or LB). A single V_{DET} output voltage, representing the magnitude of the output power in a linear V/V relationship, is provided at the V_{DET} port of the SKY77529.

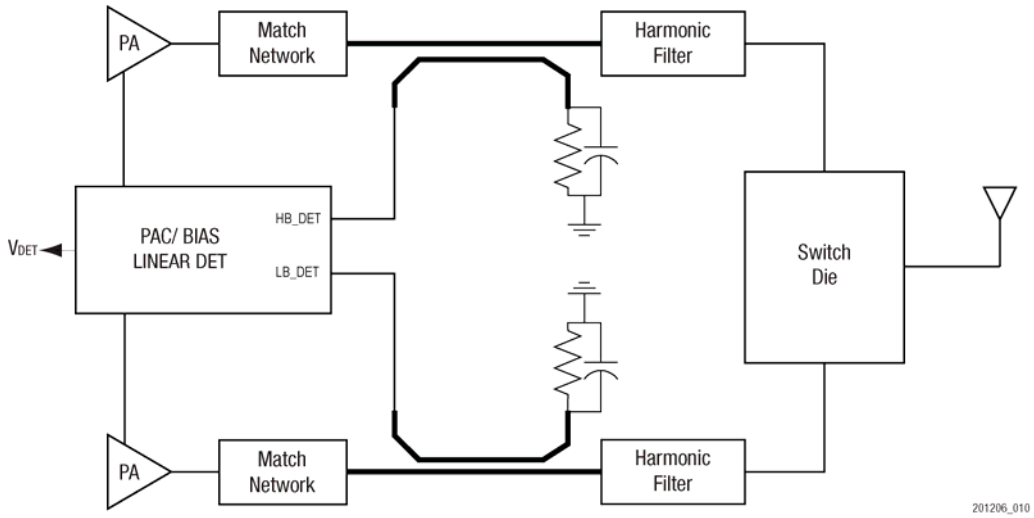

Figure 11. Linear Detector/Coupler Interface Block Diagram

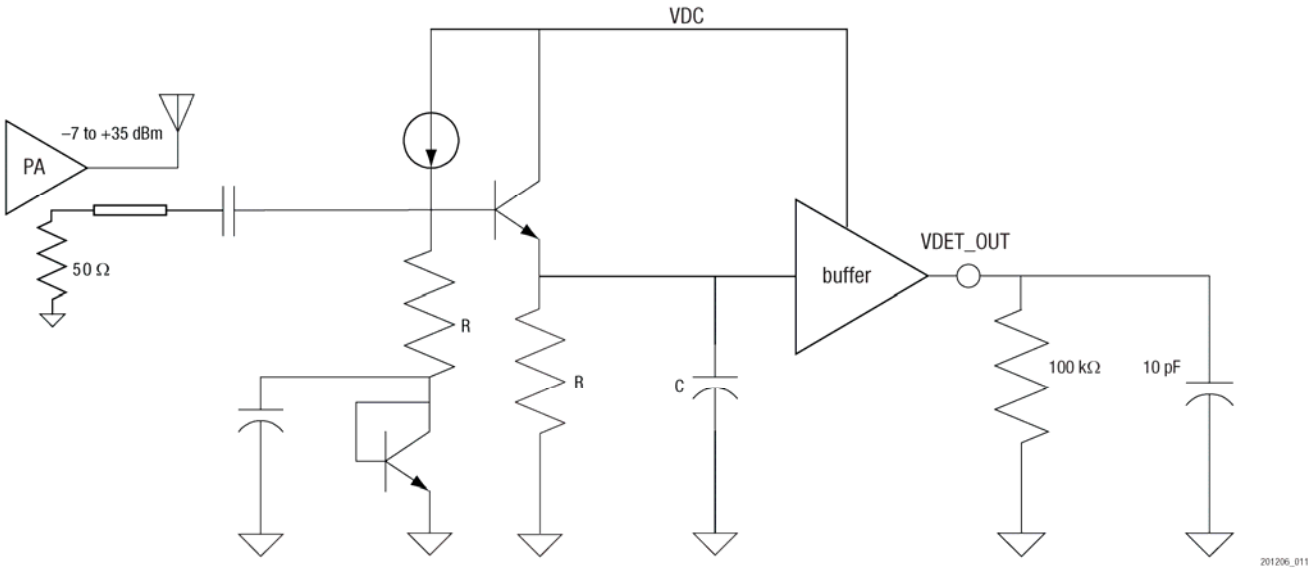

Figure 12. Linear Detector Block Diagram

SKY77529 Test Fixture

The SKY77529 test fixture assembly is shown in Figure 13 and the schematic of the test fixture is shown in Figure 14. Artwork of the four layers of the test fixture assembly is shown in Figure 15 through Figure 18.

The active signal is ultimately determined by the SPI telegram applied from either the system or the Skyworks evaluation kit using the SPI interface board and software. Refer to Skyworks Application Note, *SY77529 SPI Test and Control*, Document Number 201161.

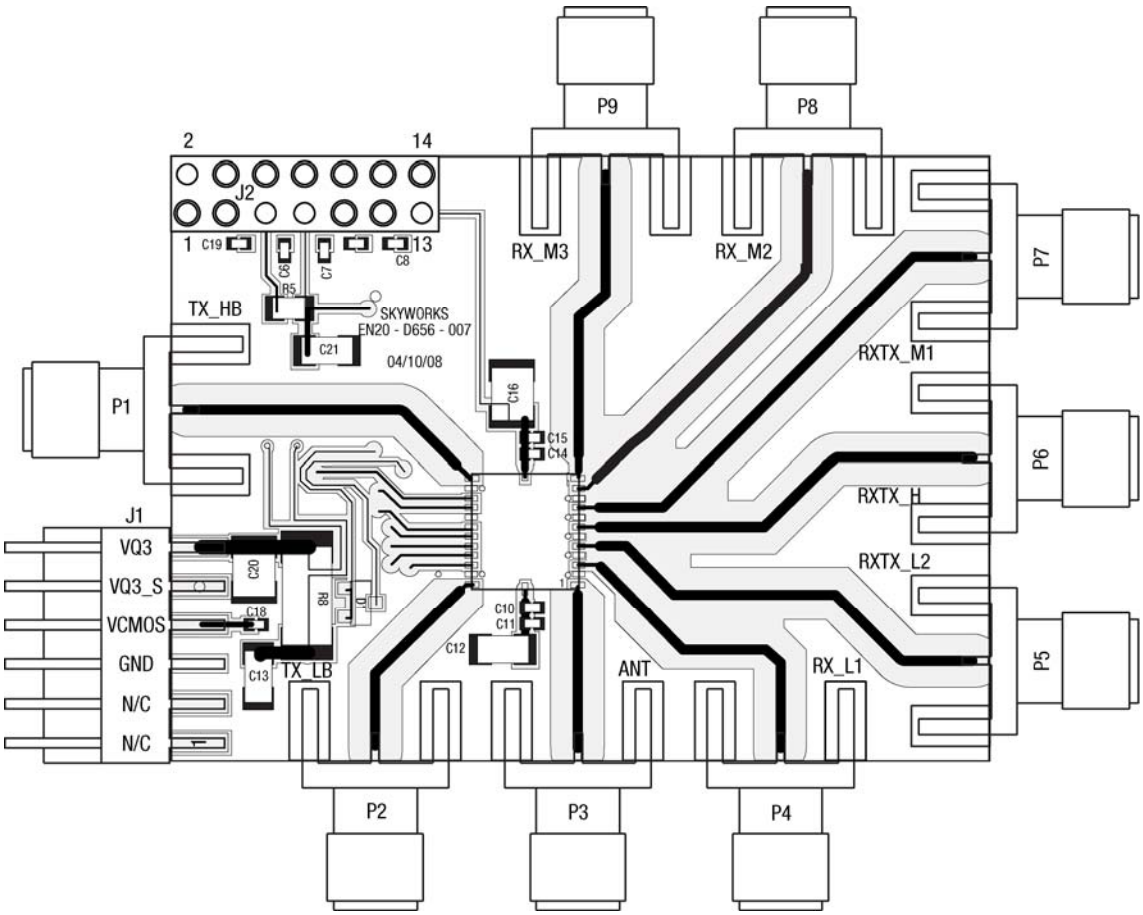

Figure 13. SKY77529 Test Fixture Assembly Diagram

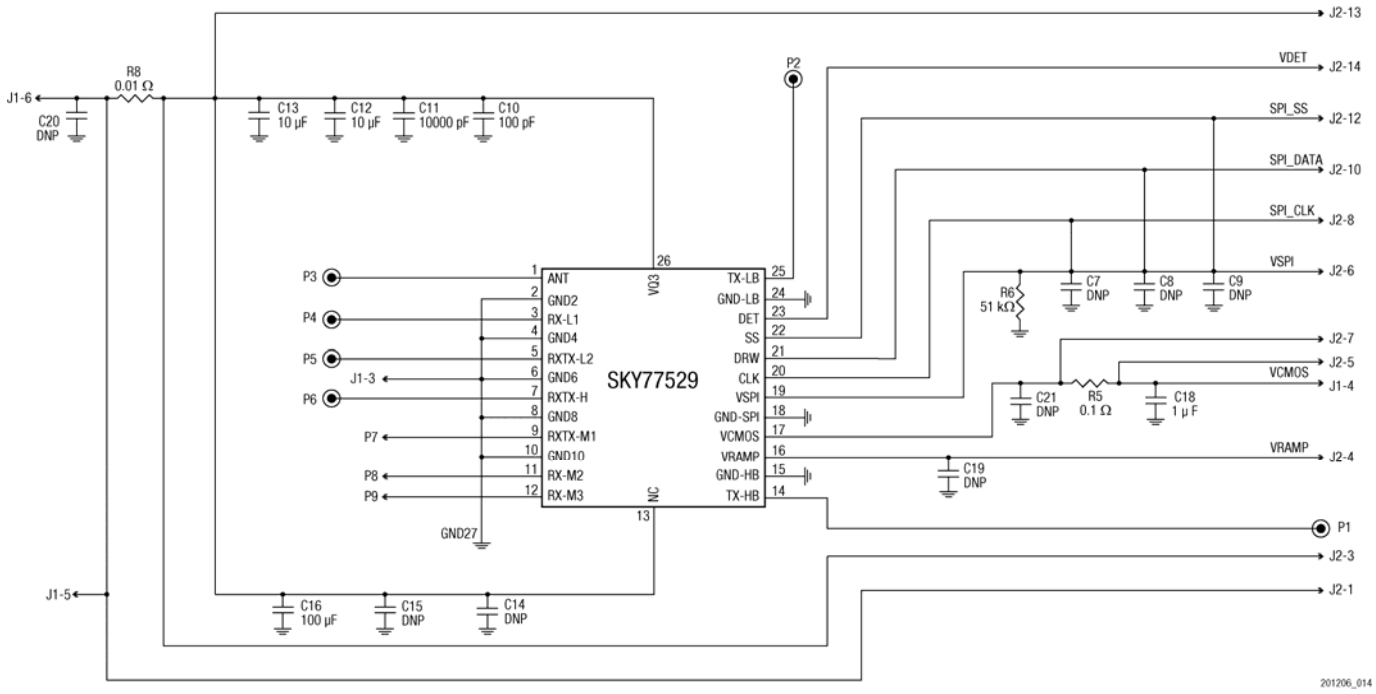

Figure 14. SKY77529 Test Fixture Assembly Schematic Diagram

Table 8. Bill of Material for SKY77529 Test Fixture

Designators	Part Number	Description
	EN20-D656-007	SKY77529 TRANSMIT MODULE TEST FIXTURE
J1	22-23-2061	MOLEX CONNECTOR
J2	90131-0127	MOLEX CONNECTOR
P1–P9	615R54-021	CONNECTOR, SMA
C10	5406R16-049	CAPACITOR, 0402, 100 pF
C11	5404R70-025	CAPACITOR, 0402, 10000 pF
C12, C13	5404R91-005	CAPACITOR, 1206, CERAMIC, 10 µF
C16	1210Y6R3107ZNE	CAPACITOR, 1206, 100 µF
C18	5404R70-034	CAPACITOR, 0402, CERAMIC, 1 uF
R5	WSL0805R1000FEA	RESISTOR, 0805, 0.1 OHMS
R6	5424R27-090	RESISTOR, 0402, 51 kOHMS
R8	WSL2512R0100FEA	RESISTOR, 2512, 0.01 OHMS

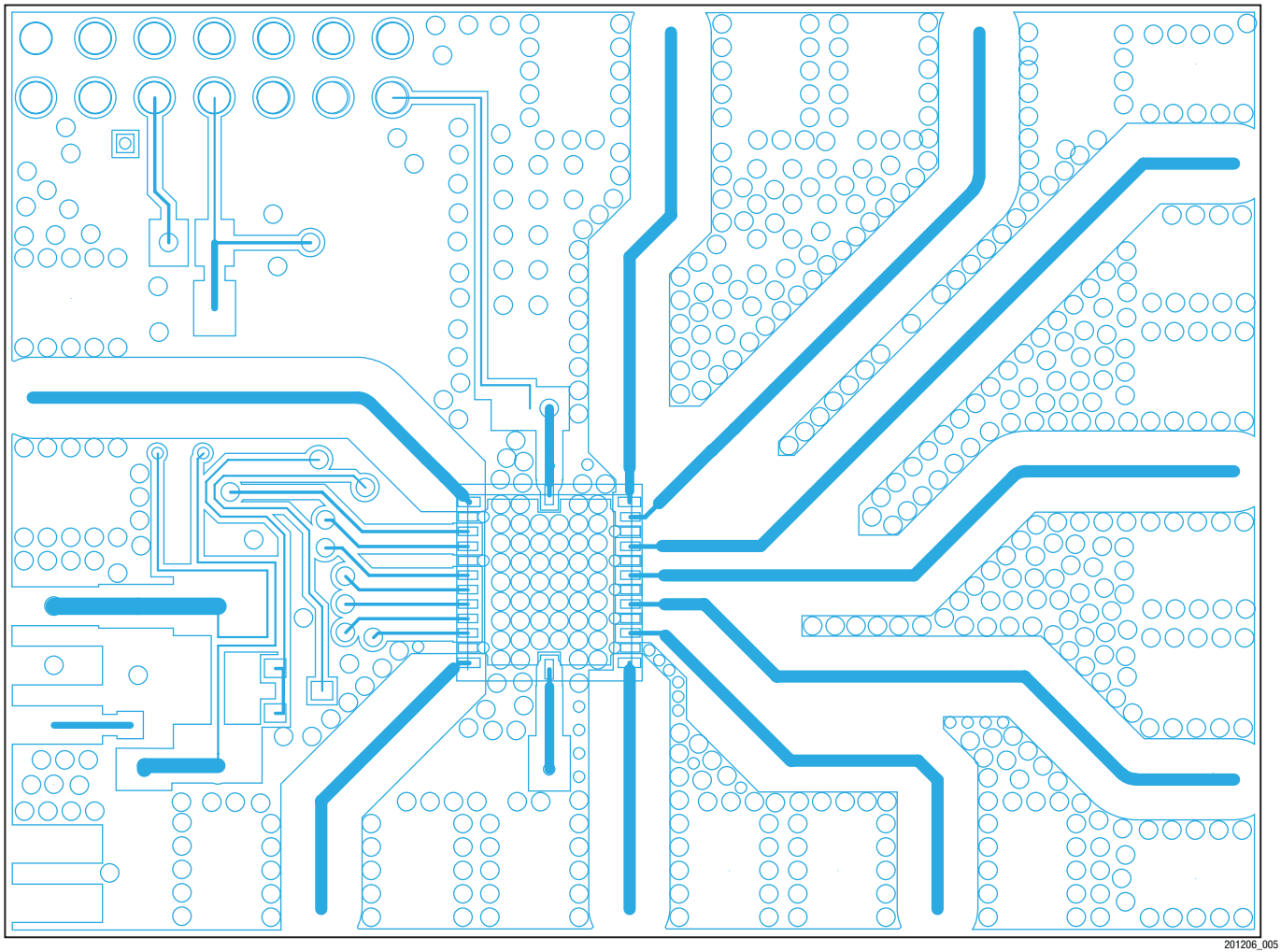

Figure 15. Test Fixture Board Layer 1

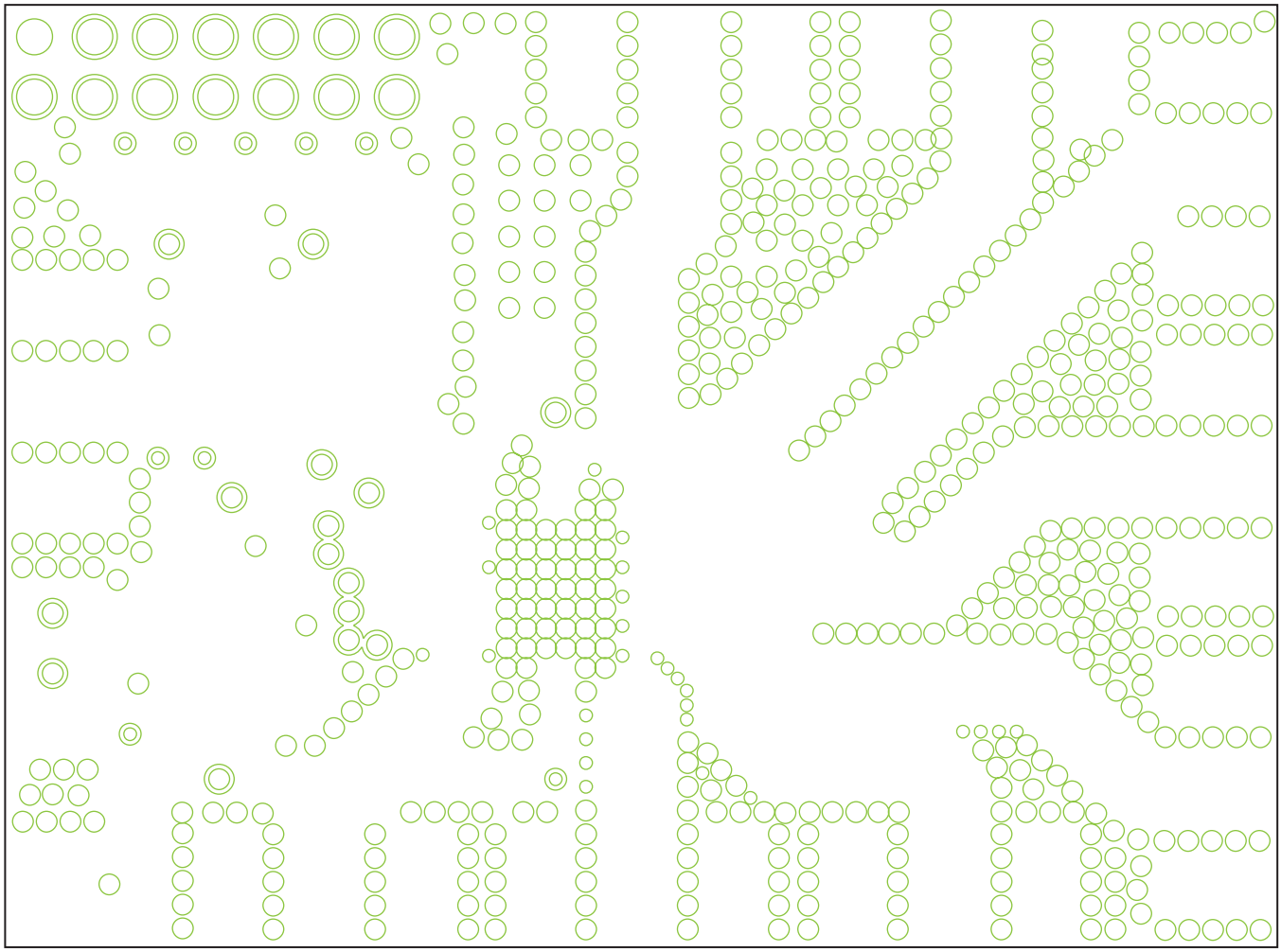

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Figure 16. Test Fixture Board Layer 2

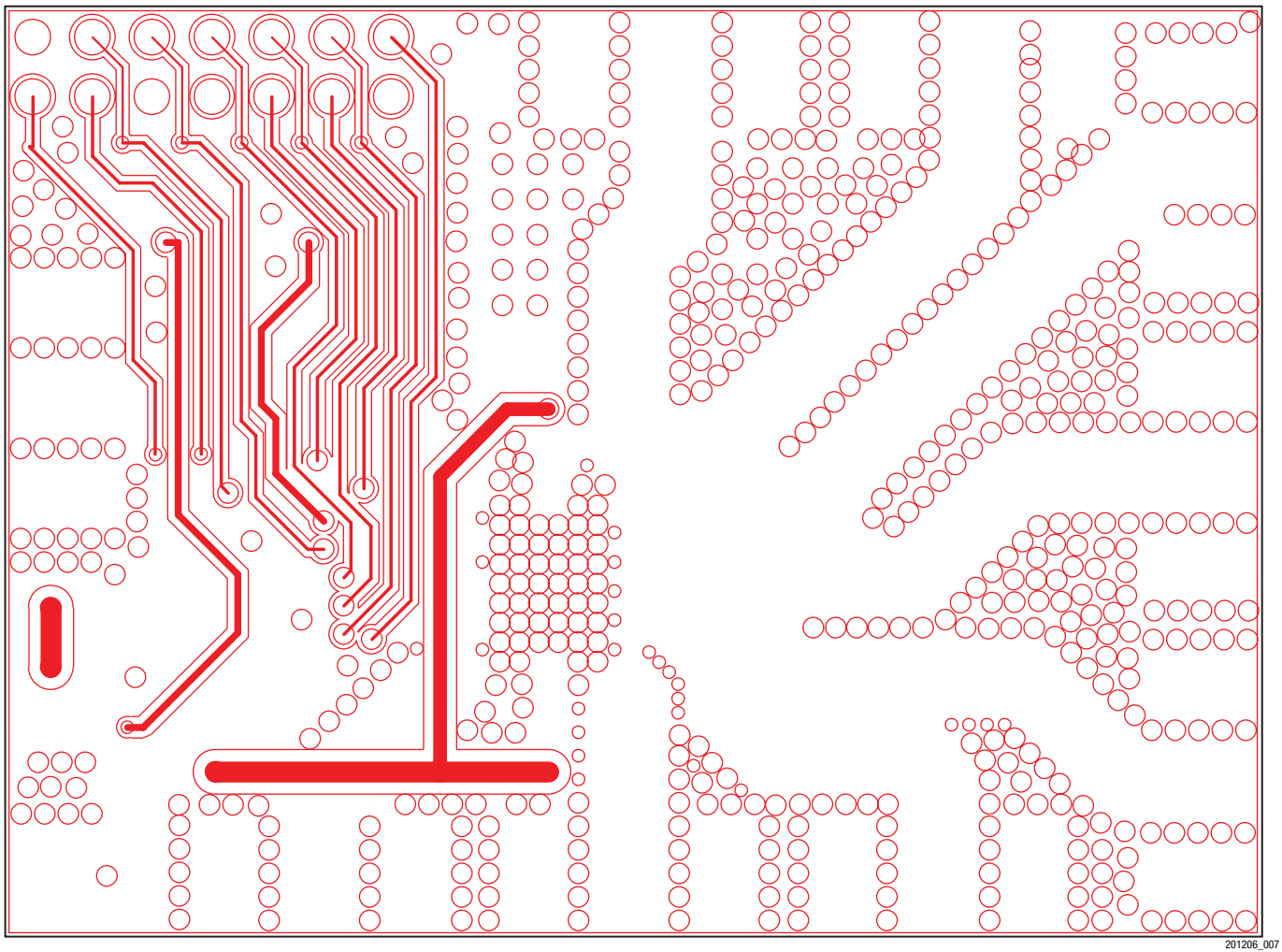

Figure 17.. Test Fixture Board Layer 3

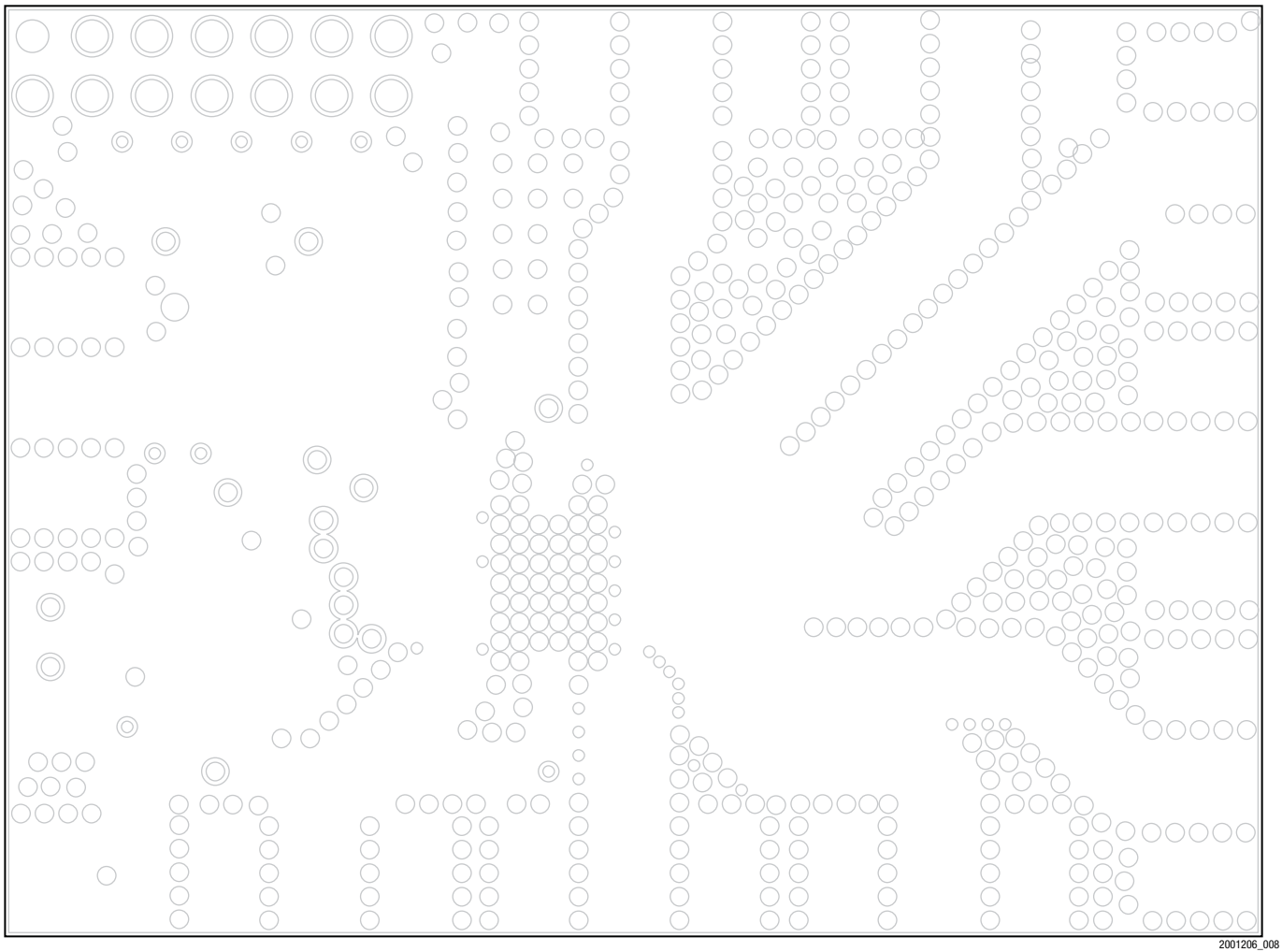

Figure 18. Test Fixture Board Layer 4

Input / Output Pad Description

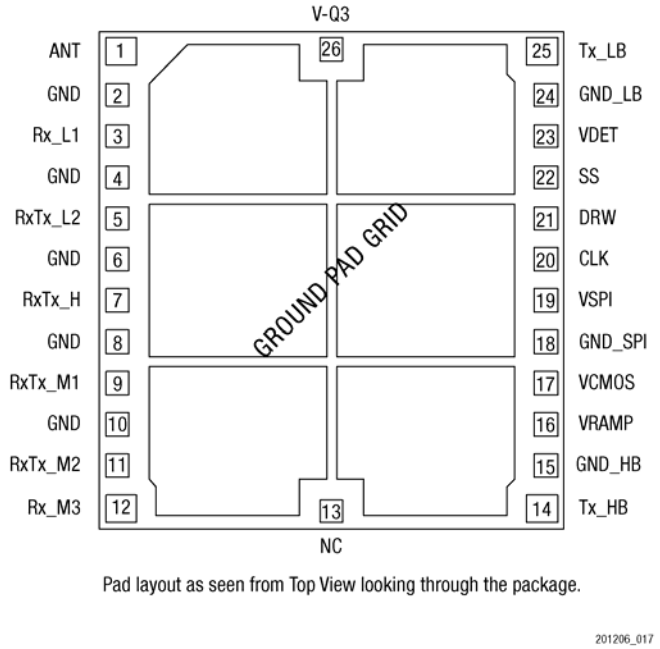

Figure 19. SKY77529 Pad Names and Configuration (Top View)

Table 9. SKY77529 Pad Names and Signal Descriptions

Pad[1]	Name	Description	Pad[1]	Name	Description
1	ANTENNA	Antenna port	17	VCMOS	Supply for CMOS controller and HBT driver stages
3	Rx_L1	Rx port GSM850/900	19	VSPI	Supply for SPI block
5	RxTx_L2	Rx port GSM850/900; Rx / Tx port WCDMA; LB port V / VIII	20	CLK	SPI signal
7	RxTx_H	Rx / Tx port WCDMA; HB port Band I	21	DRW	SPI signal
9	RxTx_M1	Rx port GSM1800/1900; Rx / Tx port WCDMA; MB port II / III	22	SS	SPI signal
11	RxTx_M2	Rx port GSM1800/1900; Rx / Tx port WCDMA bands V, VIII	23	DET	Output Detector Voltage
12	Rx_M3	Rx port GSM1800/1900	25	Tx_LB	Tx input GSM/EDGE low band
14	Tx_HB	Tx Input GSM / EDGE HB	26	VQ3	Supply for HBT output stages
16	VRAMP	Input voltage ramp signal. VRAMP controls output power in GMSK mode. In 8PSK, this signal is used to improve efficiency for lower output power by changing the bias currents of amplifier stages.	GROUND PAD GRID		Ground Pad Grid is device underside

1 Pads 2, 4, 6, 8, 10, 15, 18, 24 are GROUND pads. Pad 13 is No Connect (internal)

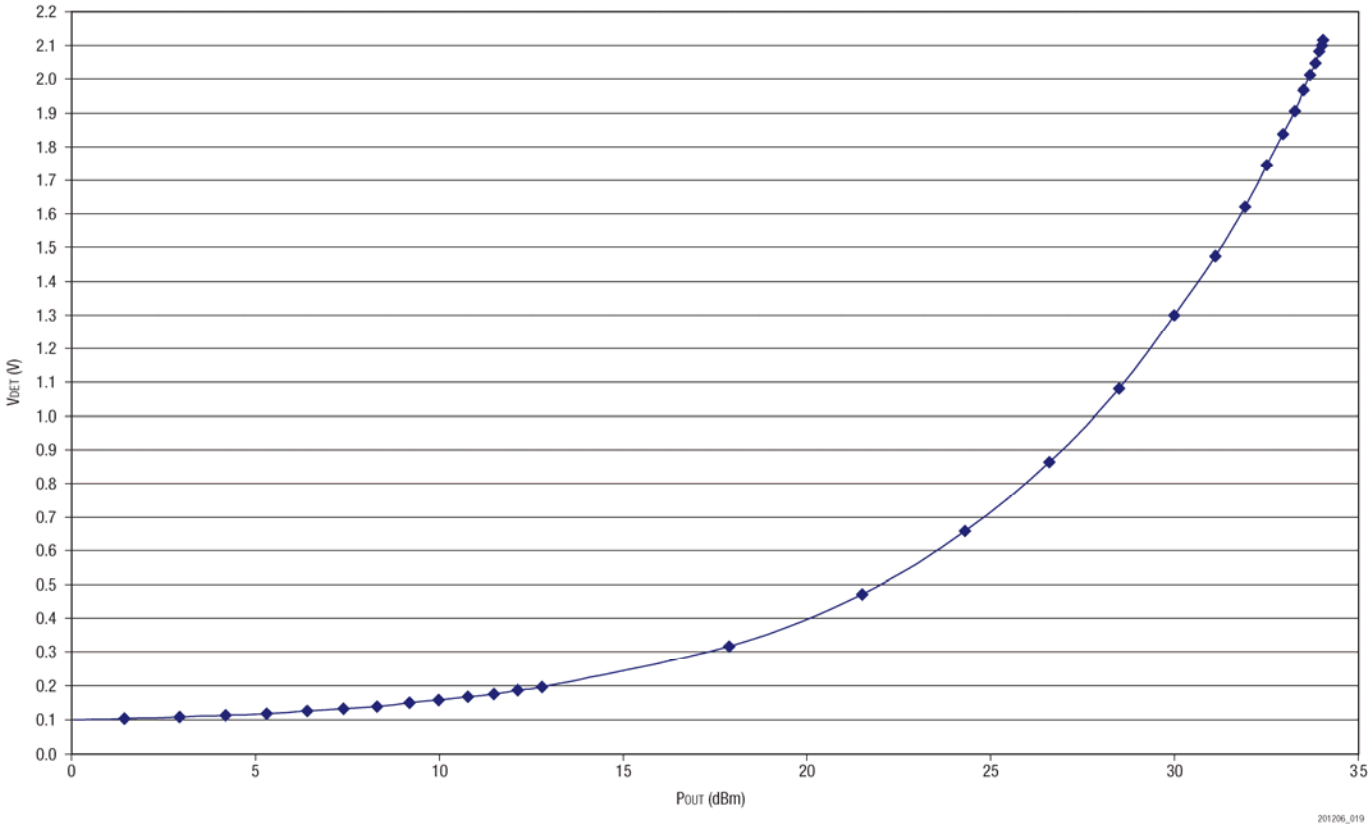

Figure 20. V_{DET} vs. P_{OUT} – 915 MHz

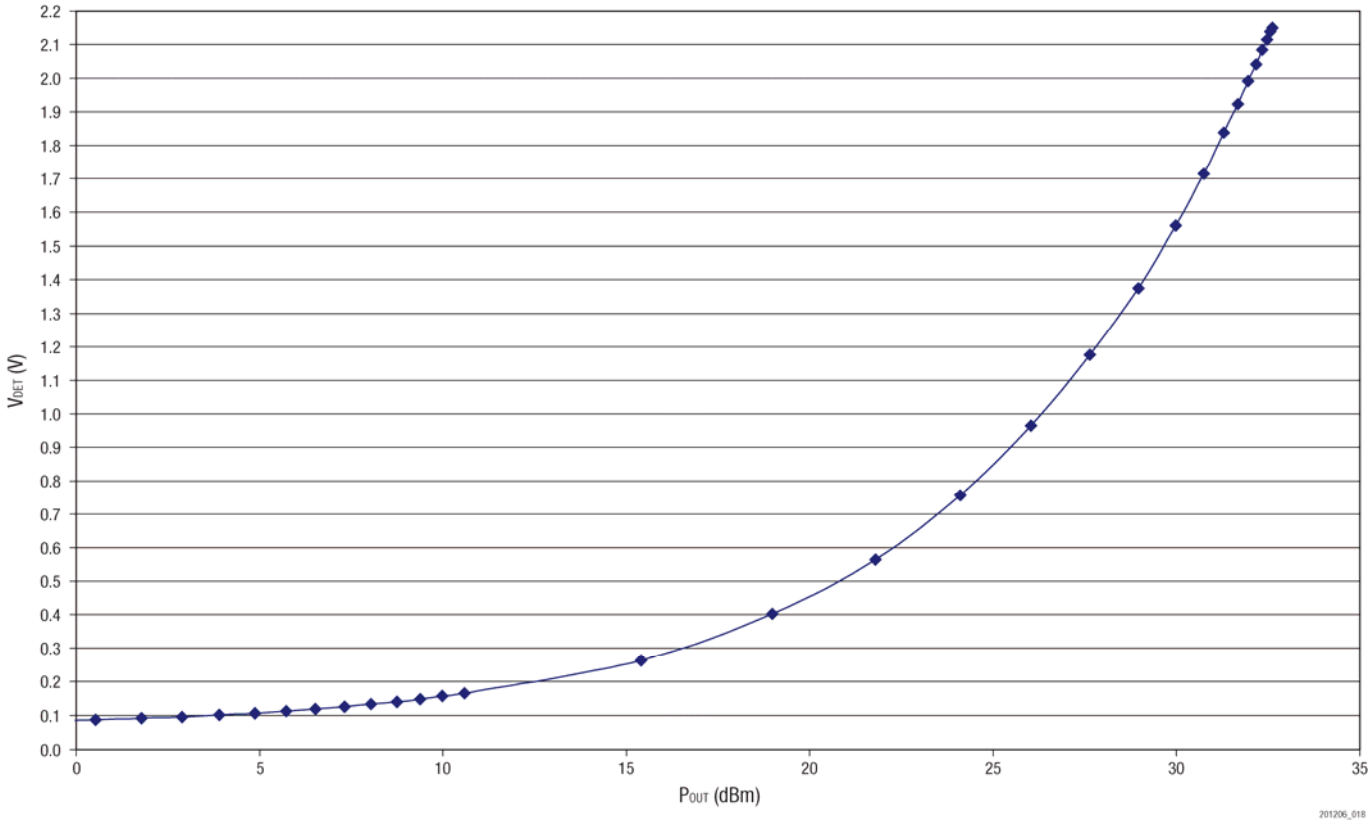

Figure 21. V_{DET} vs. P_{OUT} – 1910 MHz

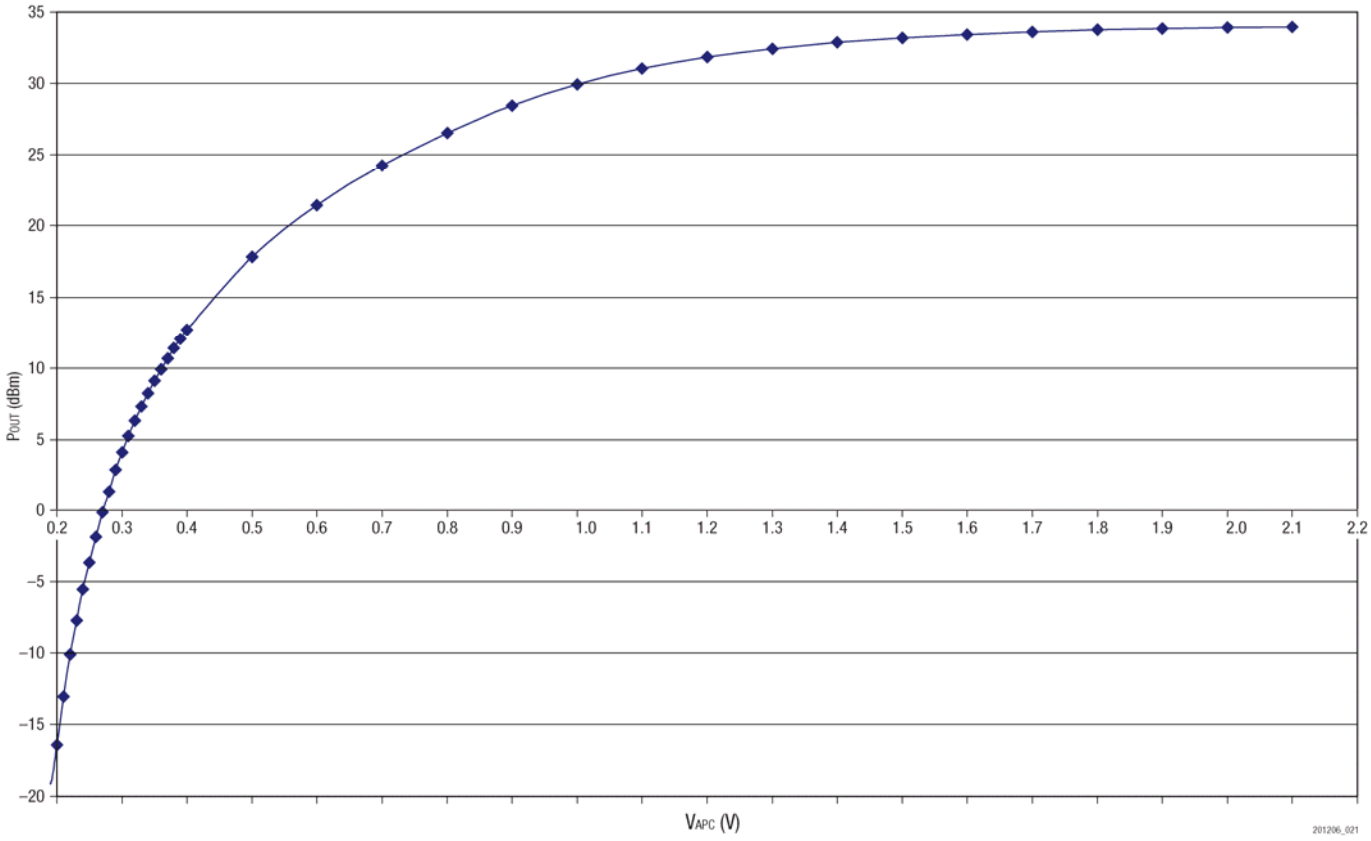

Figure 22. POUT vs. VAPC – 915 MHz

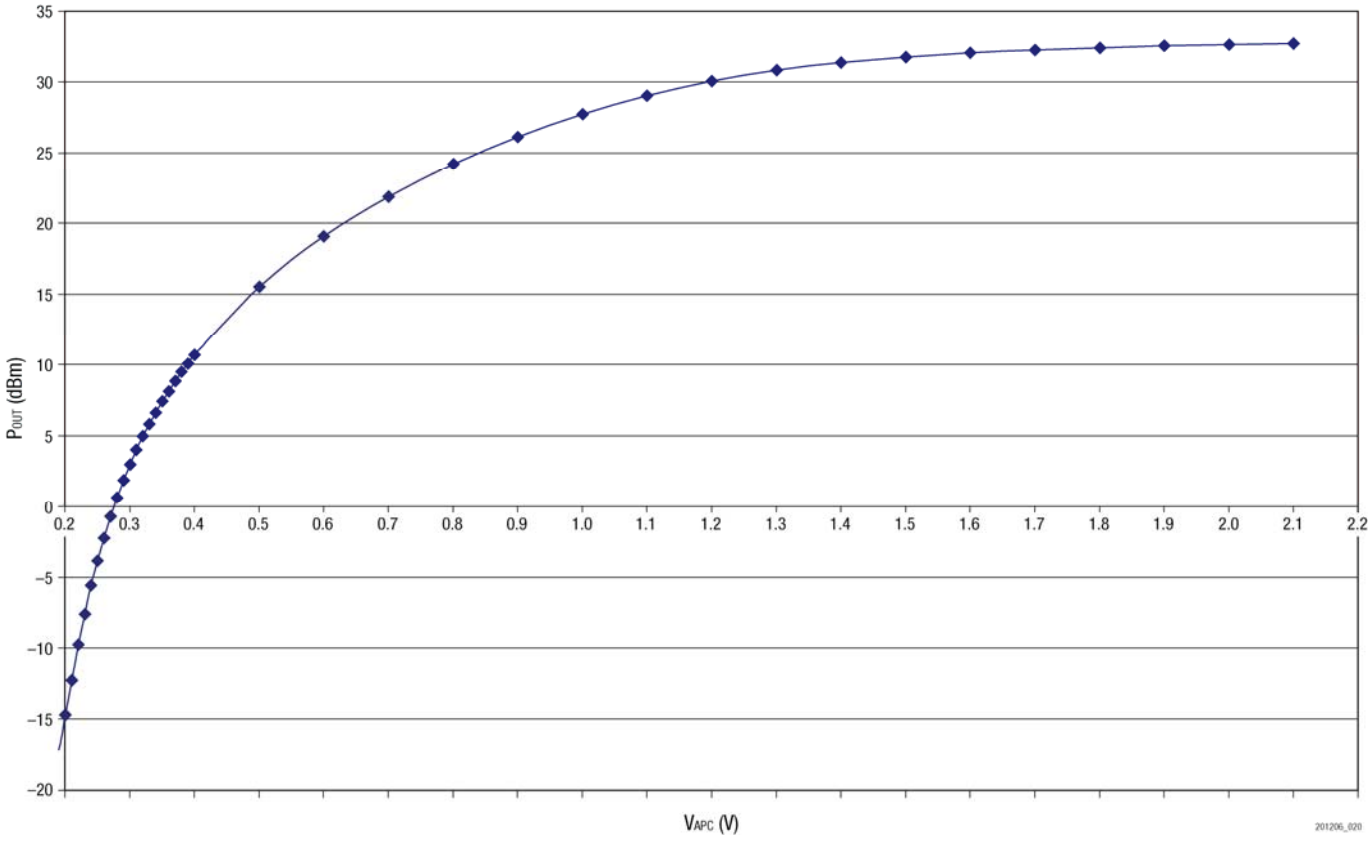

Figure 23. POUT vs. VAPC – 1910 MHz

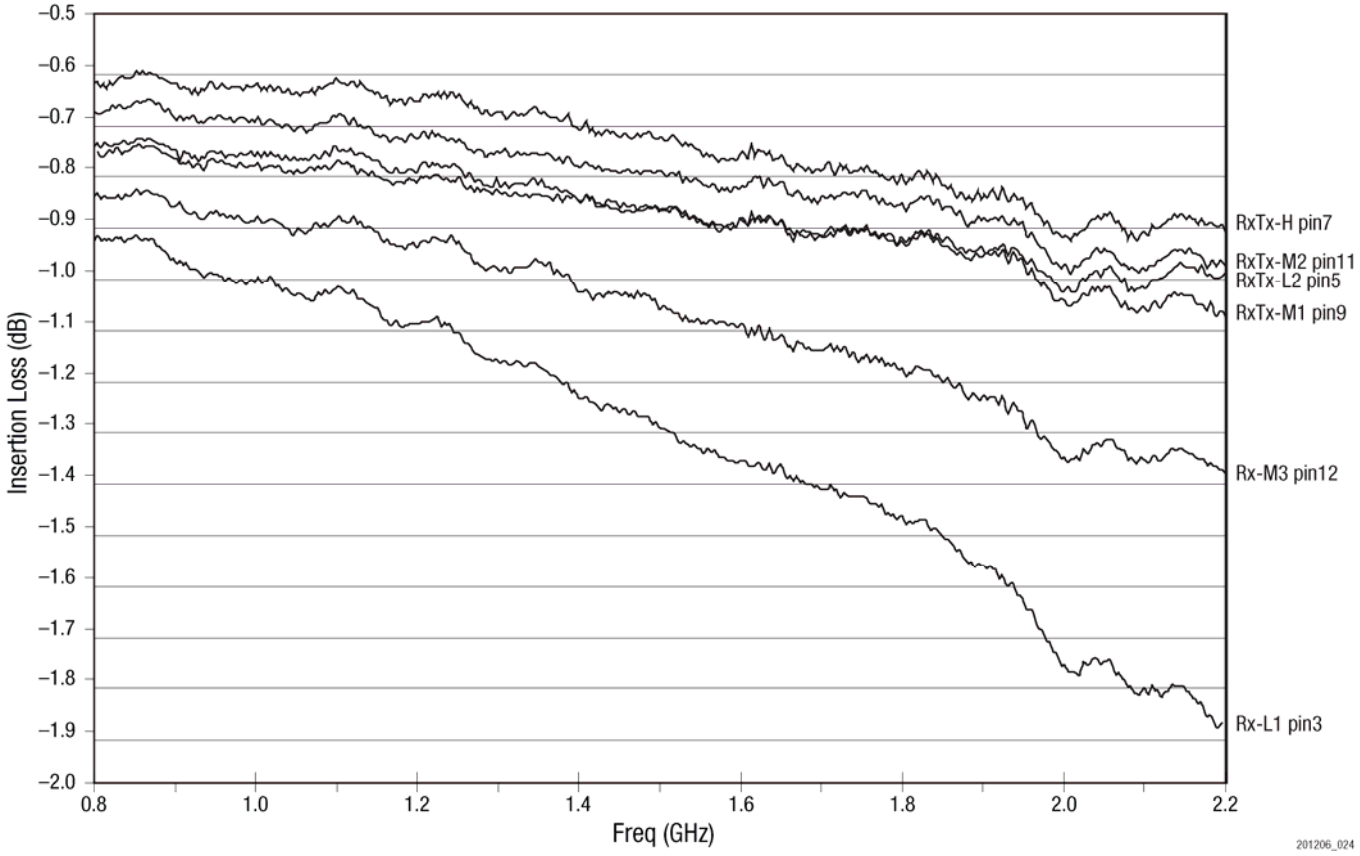

Figure 24. Rx Port Insertion Loss

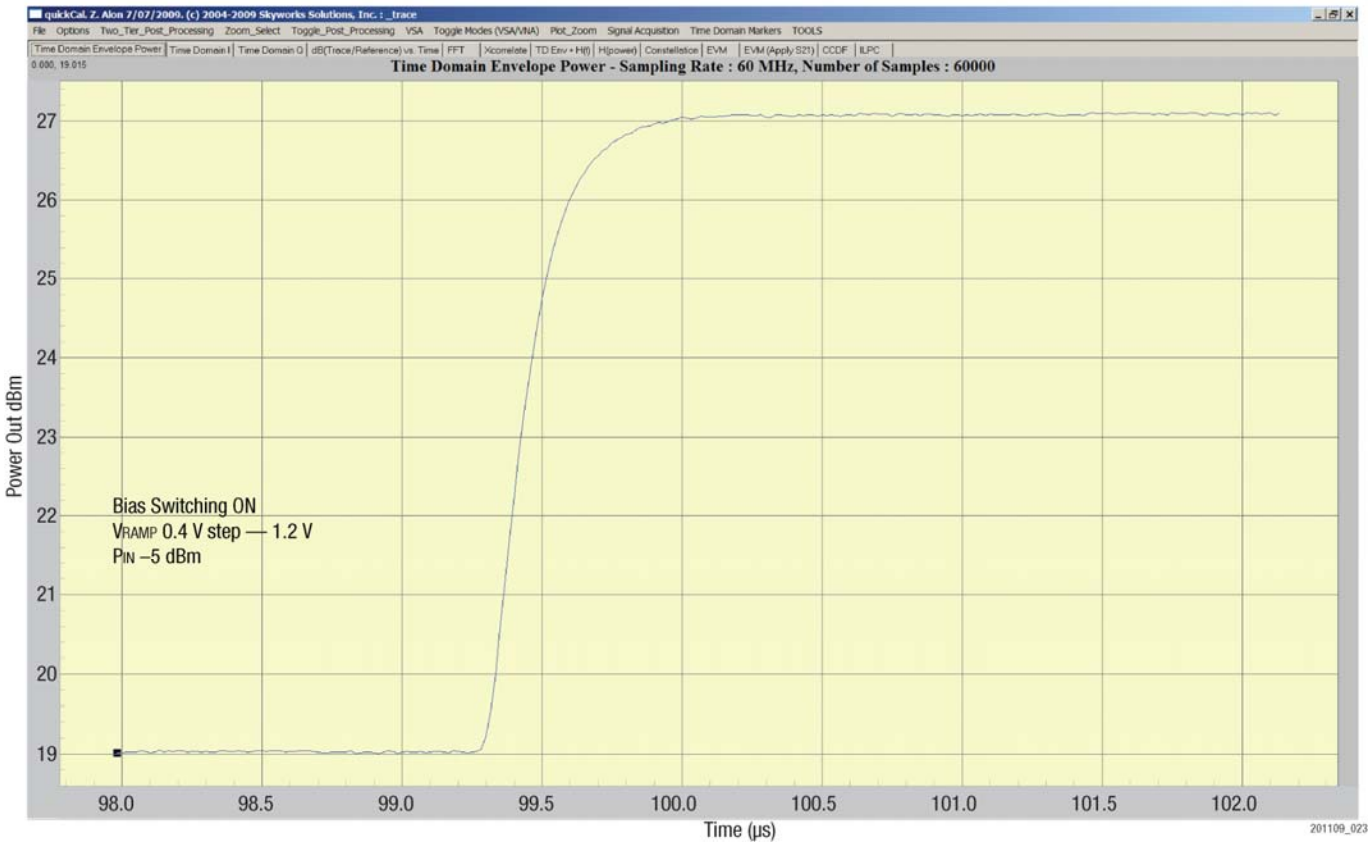

Figure 25. EDGE Bias Switch On Time

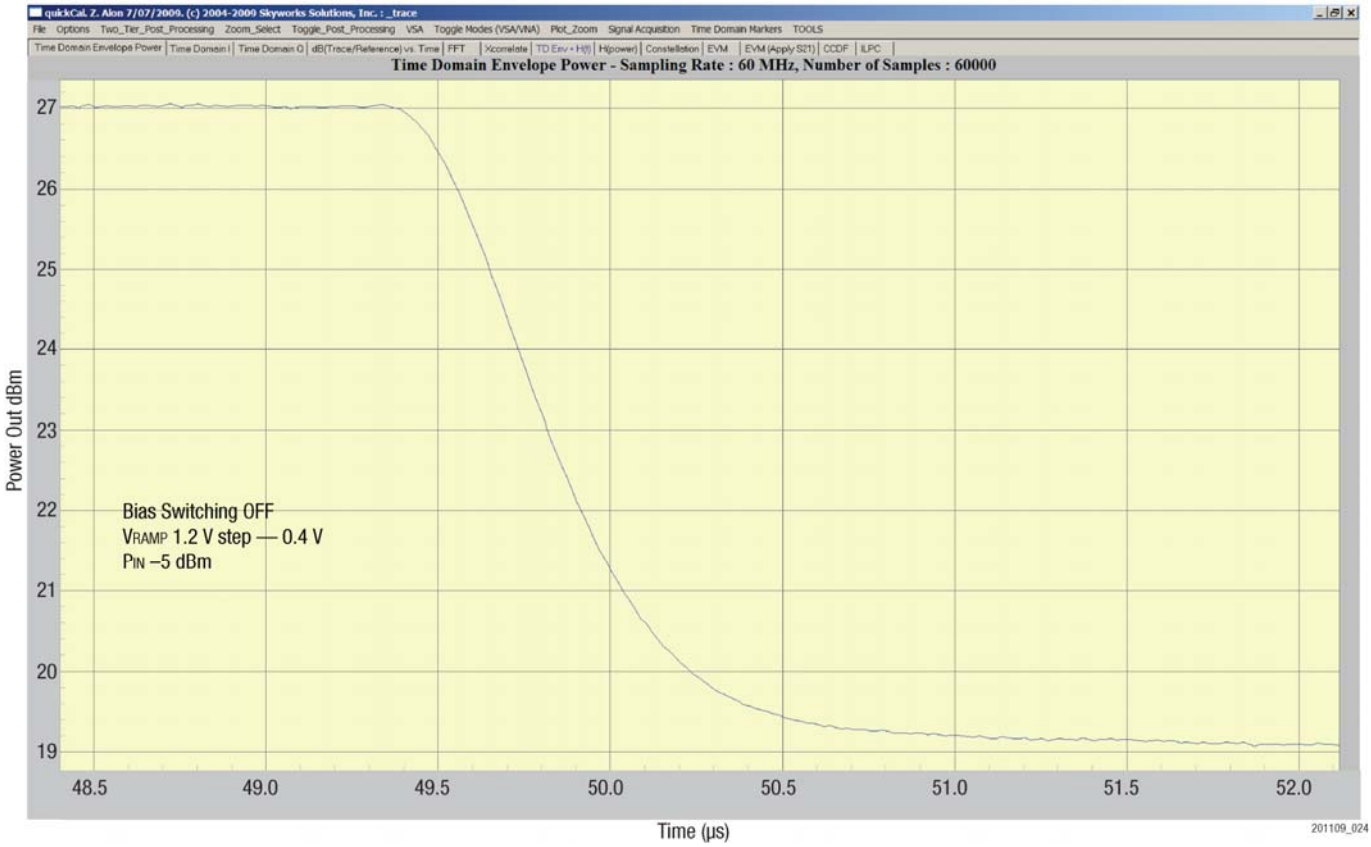

Figure 26. EDGE Bias Switch Off Time

Revision History

Revision	Date	Description
A	February 10, 2010	Initial Release
B	October 22, 2010	Revise: Figures 1, 3, 4, 14, 19; Table 9; section “Layout Guidelines for Battery Bypassing” (p4) Add: Sections “Antenna Port ESD Network” and “Rx Port DC Block” (p4)

References

Skyworks Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752

Skyworks Application Note: SKY77529 SPI Test and Control, Document Number 201161

Skyworks Data Sheet SKY77529 Rx-Tx Front-End Module for Dual-Band GSM / GPRS / EDGE, Document Number 201008